



BD21001

32W HIGH-VOLTAGE, ADJUSTABLE NON-ISOLATED DC/DC CONVERTER

$12V_{IN}$, $0V_{OUT}$ to $400V_{OUT}@80mA$

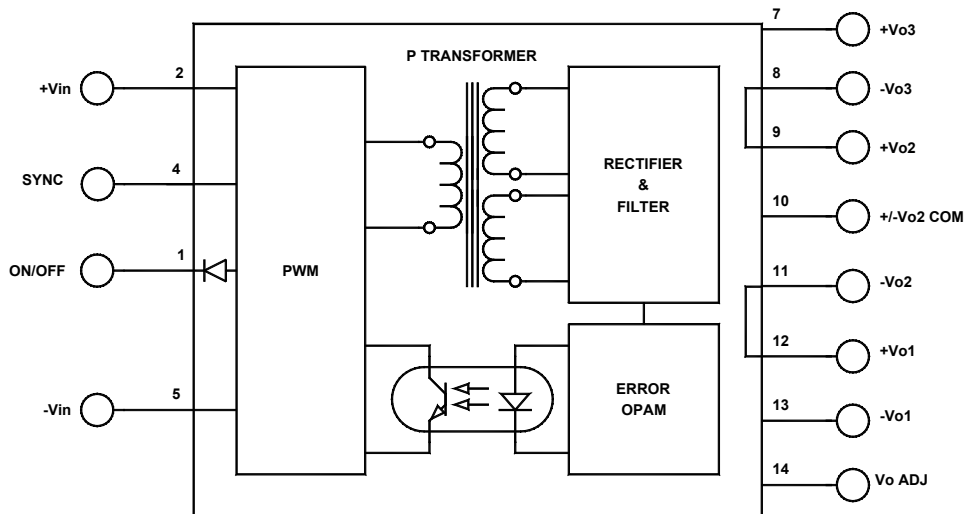
Key Features

- 85% efficiency
- 0V to 400V adjustable
- Soft start
- Input LC filter
- Short circuit
- Six-sided EMI shielding



Functional Description

The BD21001 is a 32W high-voltage, adjustable, non-isolated DC/DC converter in a 3.00×2.50×0.75-inch package that accepts $12V_{IN}$ and provides $0V_{OUT}$ to $400V_{OUT}@80mA$ when the V_O ADJ input is driven by a 1.25Vdc–0Vdc voltage source or with an external variable resistor from $1G\Omega$ to 0Ω . All three outputs are connected internally in series, while the load is applied between $+V_{O3}$ (Pin 7 positive) and $-V_{O1}$ (Pin 13 negative). The converter will charge an output capacitor of $500\mu F@400Vdc$ in 3 to 5 seconds.



Typical Block Diagram

Unless otherwise specified, all parameters are given under typical +25°C with nominal input voltage and under full output load conditions.

Electrical Specifications

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range		10.8	12	13.2	Vdc
Input Current, No Load			40		mA
Input Current, Full Load			3137		mA
Short Circuit Current	Input Current Limit	$I_{IN FL}$			
Input Reflected Ripple	$C_{IN} = 100\mu F$		250		mA_{PP}
Start Up Threshold		10.8			Vdc
Under Voltage Shutdown			10		Vdc
Input Filter Type	LC				
Off State Current			TBD		μA
Turn On Delay and Soft Start	$C_o = 500\mu F$, $R_L = 5K$, $V_o = 400Vdc$; See Figure 2		3	5	sec
Remote ON/OFF Control					
Converter ON	Open (Open circuit voltage at Pin 1: 10V Max.)				
Converter OFF		-0.6	0	0.2	Vdc
Logic Input Reference	-Input (Pin 5)				
Logic Compatibility	TTL Open Collector or CMOS Open Drain				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Output Voltage	Pin 7 = + V_{O3} , Pin 13 = GND (- V_{O1})	0		400	Vdc
Output Current			80		mA
Short Circuit Protection	Input current limit				
Load Step Response within 1% of V_{OUT}	50% FL to FL to 50% FL		1		mS
Turn On Delay			8		mS
Output Ripple & Noise	20MHz bandwidth, See Figure 1		± 1	± 2	% of V_{OUT}
Load Regulation	Minimum to Full Load		± 1	± 2	% of V_o
Line Regulation	Minimum to maximum input voltage		± 1	± 2	%
Temperature Coefficient	Nominal line		± 0.01	± 0.02	%/°C
Efficiency	Full Load		84		%
Transient Response	50% FL to FL to 50% FL to within 1% of V_{OUT}		200		μS

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Operating Temperature Range		-25		+60	°C
Thermal Resistance				1.2	°C/W
MTBF	per MIL-HDBK-217F (Ground benign, +25°C)		300,000		hours

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency			85		%
Switching Frequency	PWM frequencies		200		kHz

PHYSICAL CHARACTERISTICS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (L×W×H)	3.00×2.54×0.77 in. (76.20×64.52×19.43mm)				
Weight	7.48 oz. (212g)				
Case Material	Coated metal				
Case Connection	Case & header are floating and have no connection to either input or output pins				

¹ The input power may have to be recycled after thermal turn off.

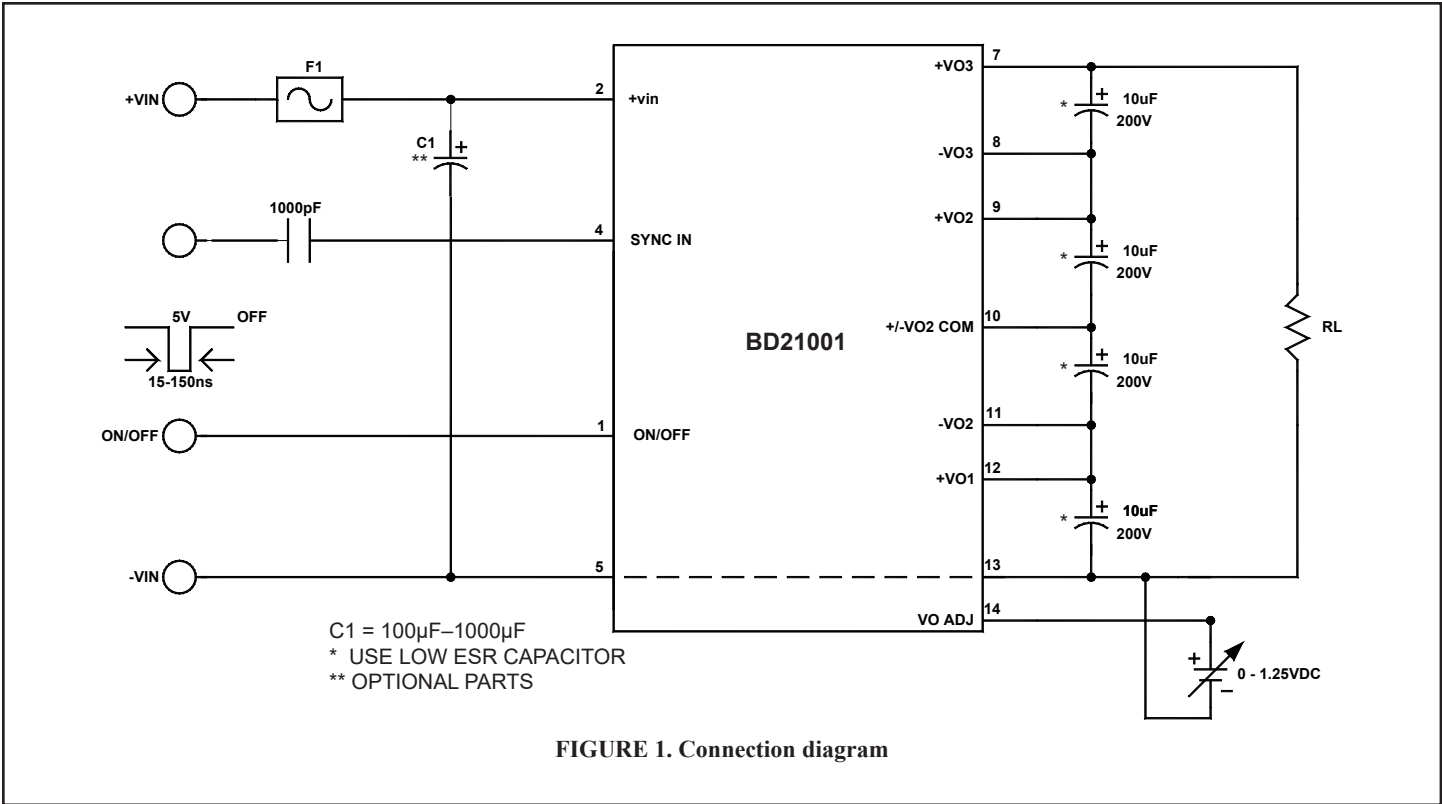
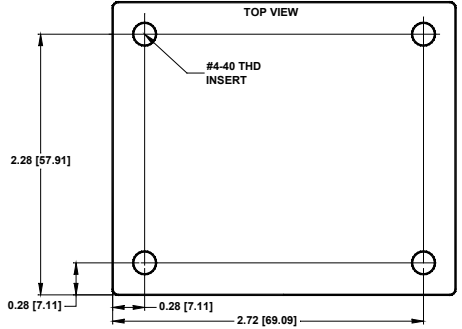
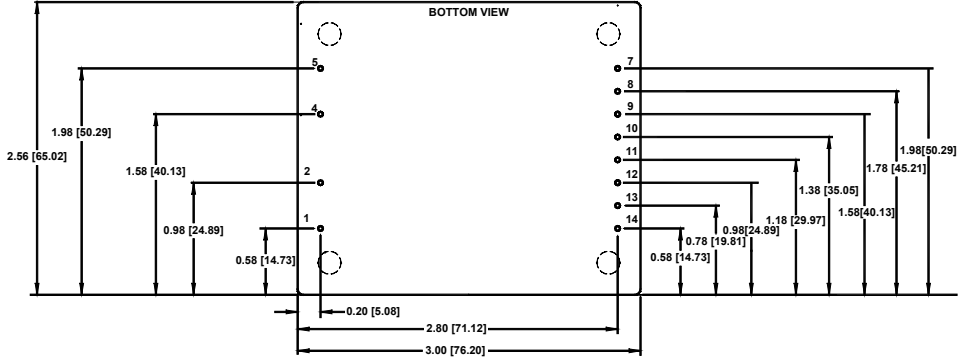
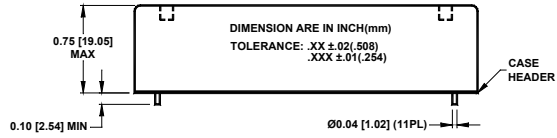


FIGURE 1. Connection diagram

MECHANICAL SPECIFICATIONS



Pin	Function	Pin	Function
1	ON/OFF	7	+V _{O3}
2	+V _{IN}	8	-V _{O3}
3	No Pin	9	+V _{O2}
4	SYNC	10	\pm V _{O2}
5	-V _{IN}	11	-V _{O2}
		12	+V _{O1}
		13	-V _{O1}
		14	V _O ADJ



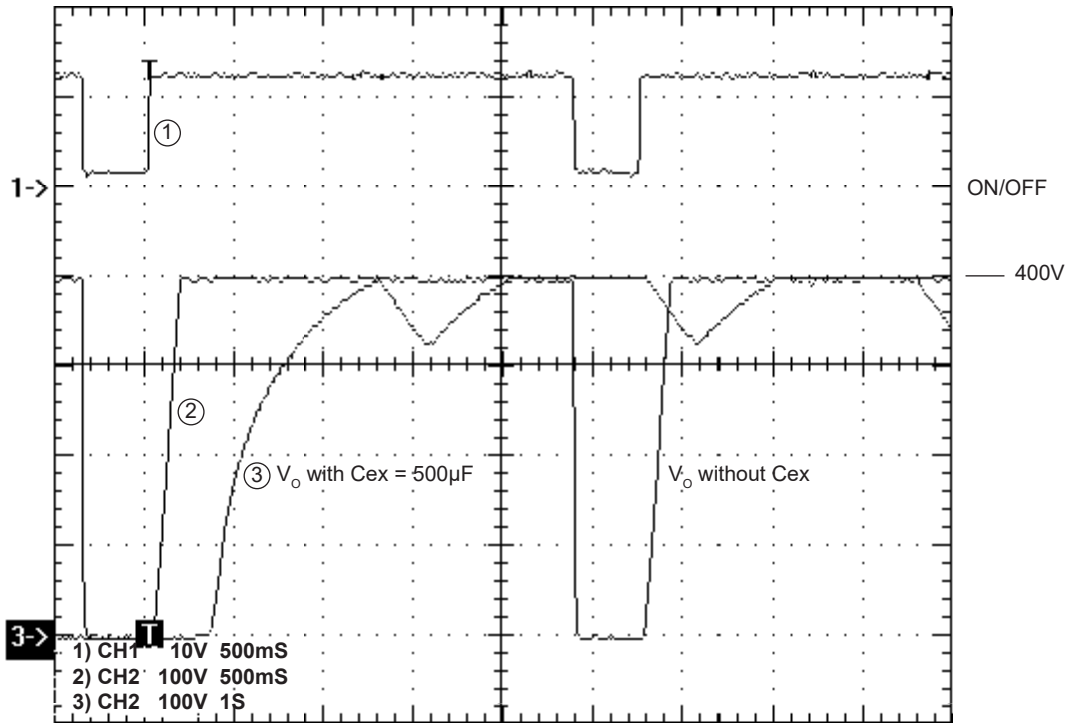


FIGURE 2. Turn on delay with soft start
 1) ON/OFF, 2) V_o without Cex, 3) V_o with Cex = 500µF

EXTERNAL SYNCHRONIZATION

The converter can be synchronized to an external clock. The external clock MUST have a higher frequency than that of the converter's switching frequency. The amplitude of the external clock pulse must be 3.7 volts or greater and its duration between 15nS to 150nS for sync pulse detection.

The circuit in Figure 3 can be used to produce a 50nS to 150nS pulse from a square wave. The circuit will be turned on by the negative edge of the square wave and will stay on for approximately 50nS (depending on the $R2 \cdot C1$ time constant) (See Figure 4).

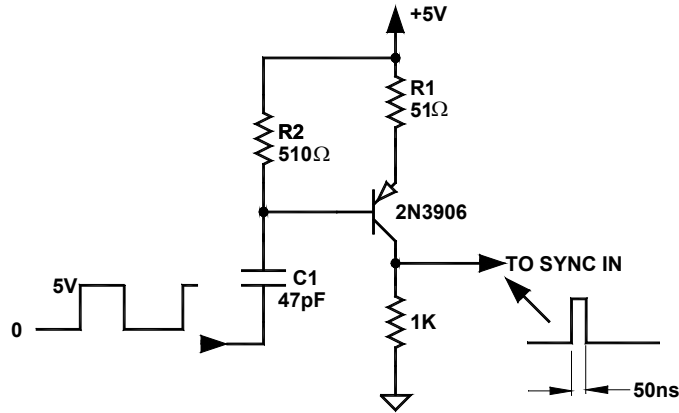


FIGURE 3. 50nS pulse generator from a square wave TTL/5V CMOS clock

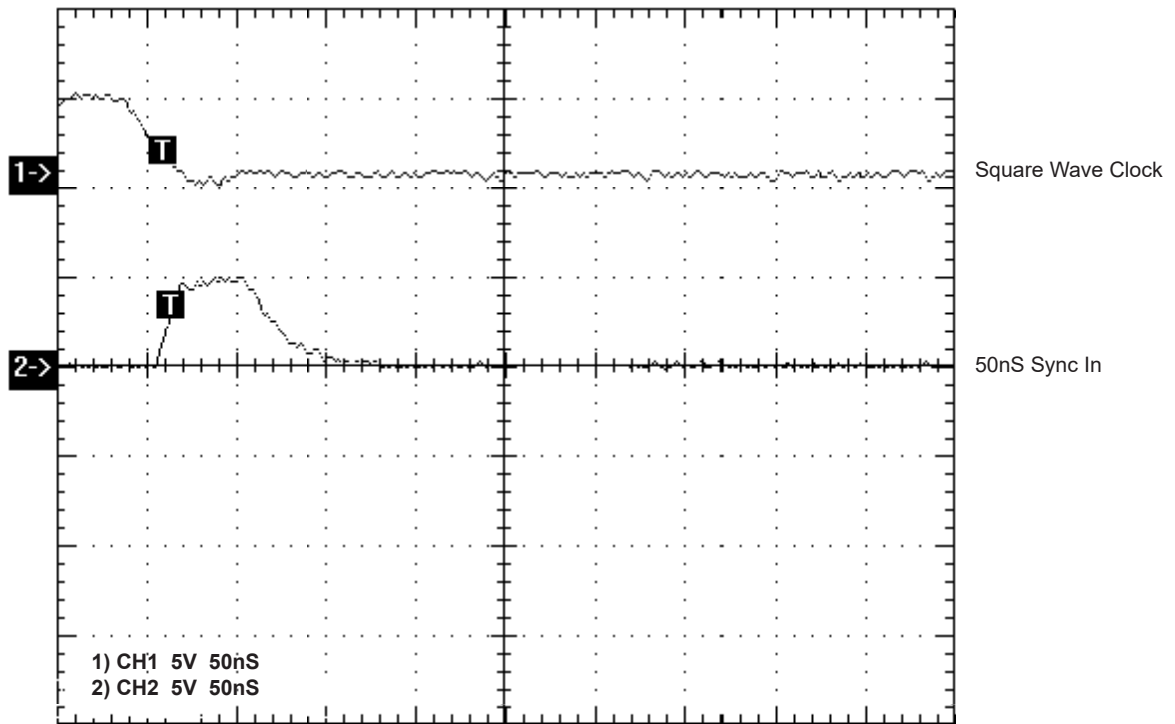


FIGURE 4. Waveforms generated from Figure 3