

PRELIMINARY



Q5001

Adjustable Output from $27V_{OUT}$ To $29V_{OUT}$
with $V_{ADJ}=5V$ to $0(\text{zero})V$ respectively
24-PIN DIP

Key Features

- Efficiency up to 83%
- 1500Vdc isolation
- Short circuit and thermal protection
- 2:1 input voltage range
- External Synchronization
- Metal case
- Six-sided shielding
- 2mA Off state current
- Industry standard pinout



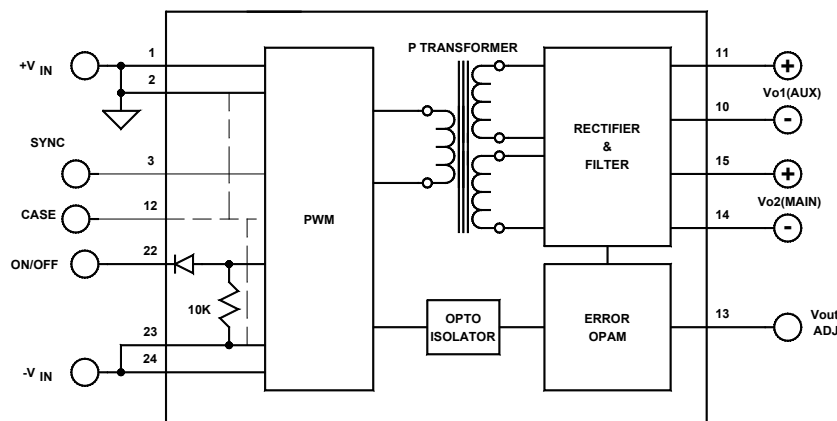
Beta Dyne is protected under various patents, including but not limited to U.S. Patent numbers: 5,777,519; 6,188,276; 6,262,901; 6,452,818; 6,473,3171.

Applications

Telcom
Computer Input/Output Boards
Instrumentation
Medical/Military

Functional Description

The Q5001 is a 2:1 input range, DC/DC Converter in a 24-Pin DIP package. The converter offers an input voltage range of $9V_{IN}$ to $18V_{IN}$, an adjustable output from $27V_{OUT}$ to $29V_{OUT}$ with $V_{ADJ} = 5V$ to $0(\text{zero})V$ respectively. Additional features include total input-to-output isolation, short circuit protection, thermal protection, metal case, and a soft start.



Typical Block Diagram

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Electrical Specifications ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, all parameters are given under typical +25°C with nominal input voltage and under full output load conditions.

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Output Short Circuit Duration	Continuous(Hiccup)				
Internal Power Dissipation				TBD	W

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range (2:1)		9	12	18	
No Load Input Current			21		mA
Full Load Input Current			.265		A
Input Filter	p Filter				μF
Reverse Polarity	External series-blocking diode				
Input Surge Current (20μS Spike)				10	A
Short Circuit Current Limit	See Short Circuit Protection		150		% I _{IN}
Off State Current			1		mA
Remote ON/OFF Control					
Supply ON	Pin 22 Open (Open circuit voltage 10V)		10		Vdc
Supply OFF	Pin 22 [Connect to -V _{IN} (Pins# 23,24)]	0	.5	.8	Vdc
Logic Input Reference	-Input for ON/OFF and SYNC				
SYNC	Referenced to -V _{IN}				
Pulse		15	200		nS
Amplitude		0	3.3	5	V

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Output Voltage Accuracy			±1	±2	%
Output Voltage		27	28	29	V
Ripple & Noise	With specified minimum output capacitors, Figure 2&3				mV
Output Current			.1		A
Line Regulation			±.5	±1	%
Load Regulation, Dual	With balanced loads		±.5	±1	%
Temperature Coefficient @ FL			0.02		%/°C
Transient Response Time	50% FL to FL to 50% FL		50	100	mS
Short Circuit Protection ¹	By input current limiting(Hiccup mode)				
Output Adjust Range	See Figure 1				

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency	V _{IN} = 12V, V _{OUT} = 28V, I _{OUT} = .10A,		86		
Isolation Voltage (1 min.), Input to Output			1500		Vdc
Isolation Voltage (1 min.), Output to Output			500		Vdc
Isolation Resistance			10 ⁹		Ω
Isolation Capacitance			1000		pF
Switching Frequency			190		kHz
Synchronization Switching Frequency			200		kHz
Turn On Delay			15	20	mS
Soft Start Time			10		mS

PHYSICAL CHARACTERISTICS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (L×W×H)	1.25×0.80×0.40 in. (31.75×20.32×10.16mm)				
Weight	0.56 oz. (15.8g)				
Case Material	Coated metal				
Shielding	Six-sided continuous				
Case Connection	Pin#12				

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Operating Temperature Range (Ambient), 24V _{IN}		-40		+60	°C
Storage Temperature Range		-60		+105	°C
Humidity	Up to 95% non-condensing				
Cooling	Free-air convection				
MTBF	per MIL-HNBK-217F (Ground benign, +25°C)		1.3x10 ⁶		hours

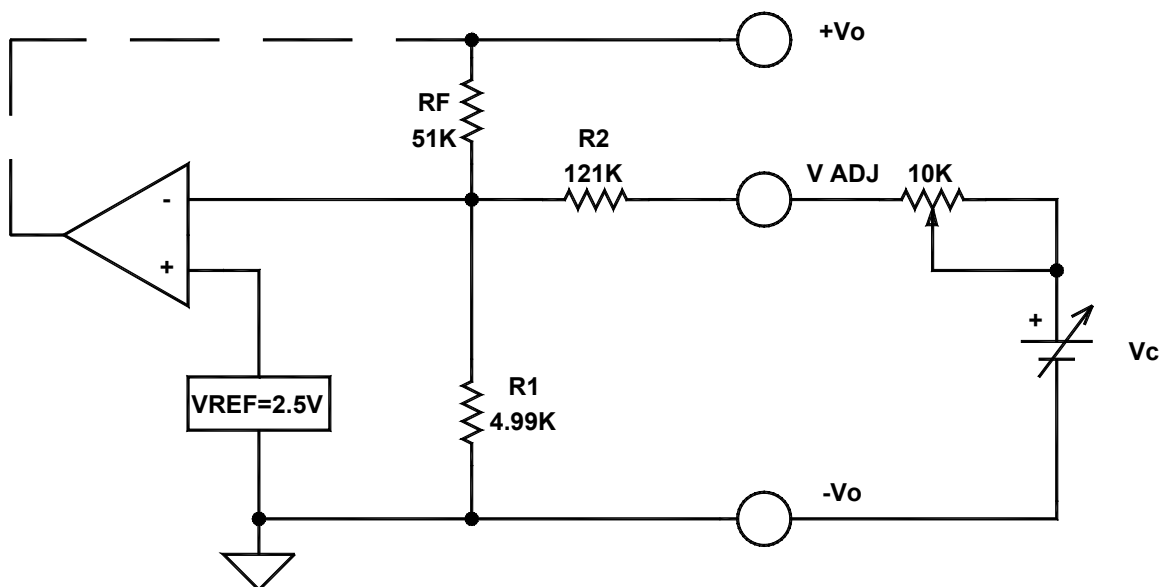


FIGURE 1. Output adjustment circuit with equations of Q5001

Maximum $R_2 = 121K + 10K$

$V_C = 0V$ to $5V$

$$V_{OUT} = V_{REF} (1 + R_F/R_1 || R_2) - (R_F/R_2) V_C$$

With $R_2 = 121K$ and $V_C = 0$

$$V_{OUT} = 2.5(1 + 51/4.79236)$$

$$V_{OUT} = 29.1048V$$

With $R_2 = 121K$ and $V_C = 5V$

$$V_{OUT} = 2.5(1 + 51/4.79236) - (51/121)V_C$$

$$V_{OUT} = 29.1048 - .4215V_C$$

$$V_{OUT} = 26.9973V$$

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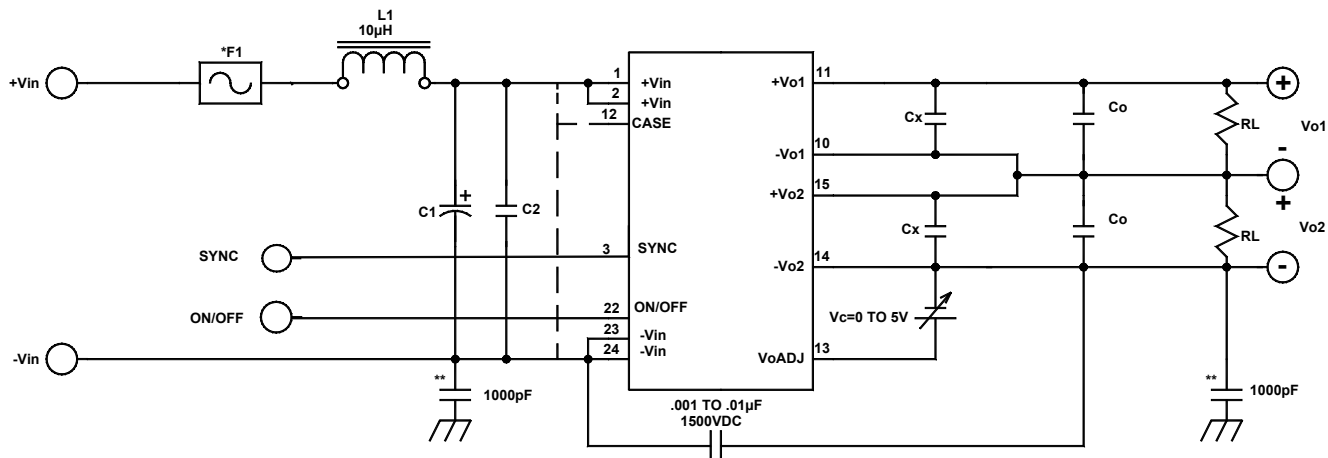


FIGURE 2. Typical connection diagram of Q5001 with external capacitors only.

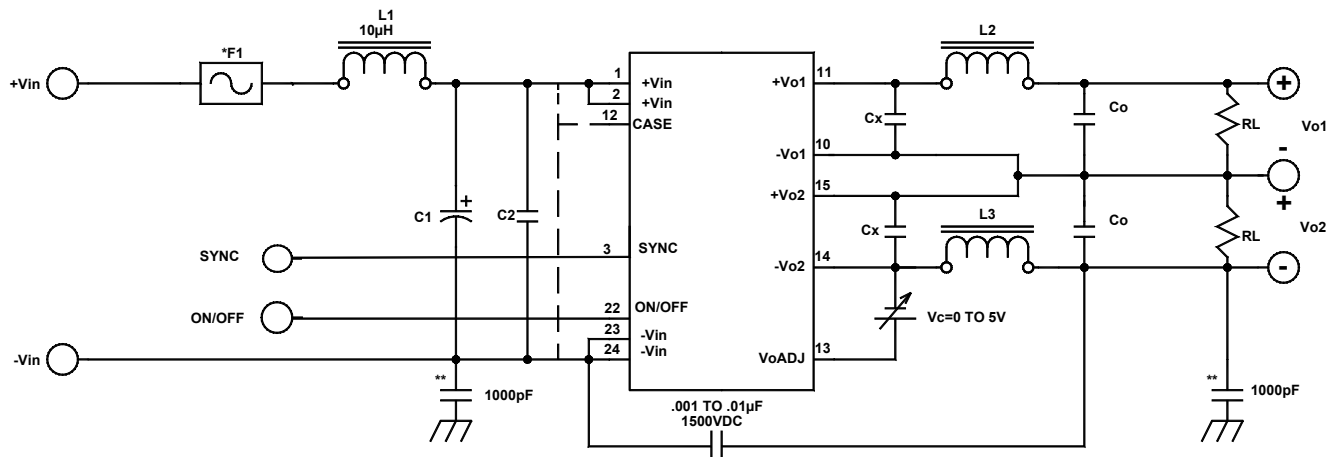


FIGURE 3. Typical connection diagram of Q5001 with external p filter

Notes: All parts below are for both diagrams, except L_2 and L_3 are only for Figure 3. Figure 3 will allow to reduce the output ripple of the converter to 1mV pk-pk or less.

$C_1 = 33\mu\text{F}@25\text{V}$ Tantalum Vishay Sprague

$C_2 = 10\mu\text{F}@25\text{V}$ Ceramic TDK

$C_x = 22\mu\text{F}@50\text{V}$ Ceramic TDK

$C_o = 22\mu\text{F}@50\text{V}$ Ceramic TDK

$L_2, L_3 = 6.8\mu\text{H}$ Central Technologies

*F1 is a 1A slow blow fuse

Part# 594D336X9025D2T

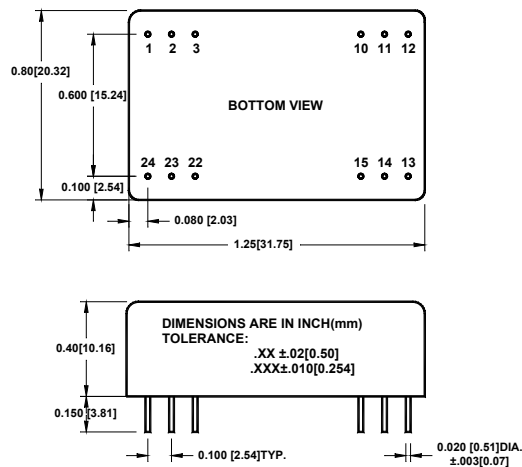
Part# C4532X7R1E106K250KA

Part# TDKCKG57NX7S1H226M

Part# TDKCKG57NX7S1H226M

Part# CTG54F-6R8M or equivalent

MECHANICAL SPECIFICATIONS



Pin	Dual
1	+V _{IN}
2	+V _{IN}
3	SYNC
10	-V _{O1}
11	+V _{O1}
12	CASE PIN
13	V _{OUT} ADJ
14	-V _{O2}
15	+V _{O2}
22	ON/OFF
23	-V _{IN}
24	-V _{IN}

EXTERNAL SYNCHRONIZATION

The SYNC pin can be used to synchronize the internal oscillator to an external clock. An open drain output is the recommended interface between the external clock to the Q5001 SYNC pin as shown in Figure 4. The clock pulse width must be greater than 15ns. The external clock frequency must be greater than the frequency of the Q5.

Multiple Q5 converters can be synchronized together simply by connecting the converters SYNC pins together as shown in Figure 5. Care should be taken to ensure the ground potential differences between the converters are minimized. In this configuration, all the converters will be synchronized to the highest frequency device. The SYNC pin is a CMOS buffer with pull-up current limited to 200 micro amps. If the external device forces the SYNC pin low before the internal oscillator ramp completes its charging cycle, the ramp will reset and another cycle begins. If the SYNC pins of multiple Q5001 converters are connected together, the first SYNC pin that pulls low will reset the oscillator ramp of all the other converters. All converters will operate in phase when synchronized using the SYNC feature. Up to five devices can be synchronized using this method.

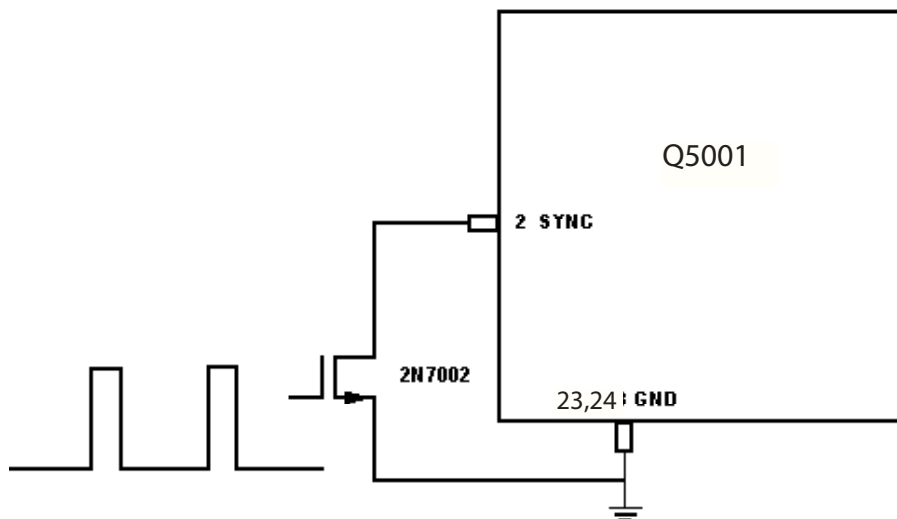


FIGURE 4. SYNC from external clock

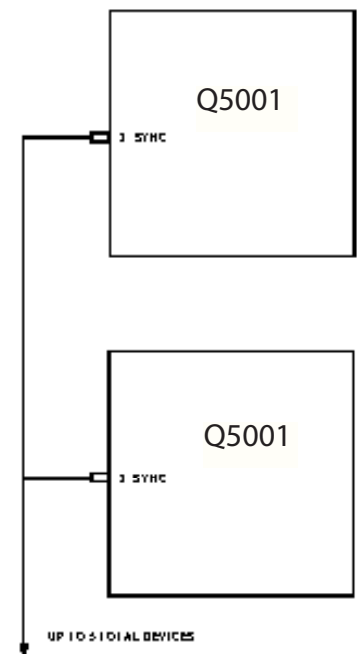


FIGURE 5. SYNC of multiple devices