PRELIMINARY

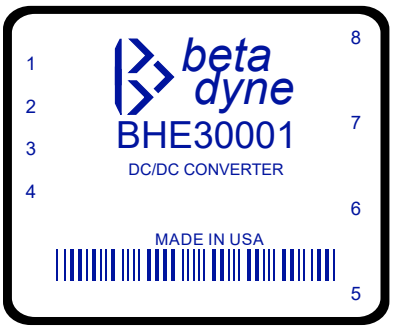
BHE30001 DC/DC CONVERTER

V_{OUT}=±5.7V@±500mA, V_{IN}=9-36V,4:1 Input Range

US Patent 5,777,519

Key Features

- Wide input voltage range 4:1
- Less than 20mV output noise
- Efficiency up to 84%
- Six-sided shielding
- Soft start
- Hiccup short circuit protection
- Adjustable output
- 2.5mA off state current
- 50µS transient response
- Industry standard pinouts
- External synchronization



Beta Dyne is protected under various patents, including but not limited to U.S. Patent numbers: 5,777,519; 6,188,276; 6,262,901; 6,452,818; 6,473,3171.

Applications

High-Resolution Data Converters

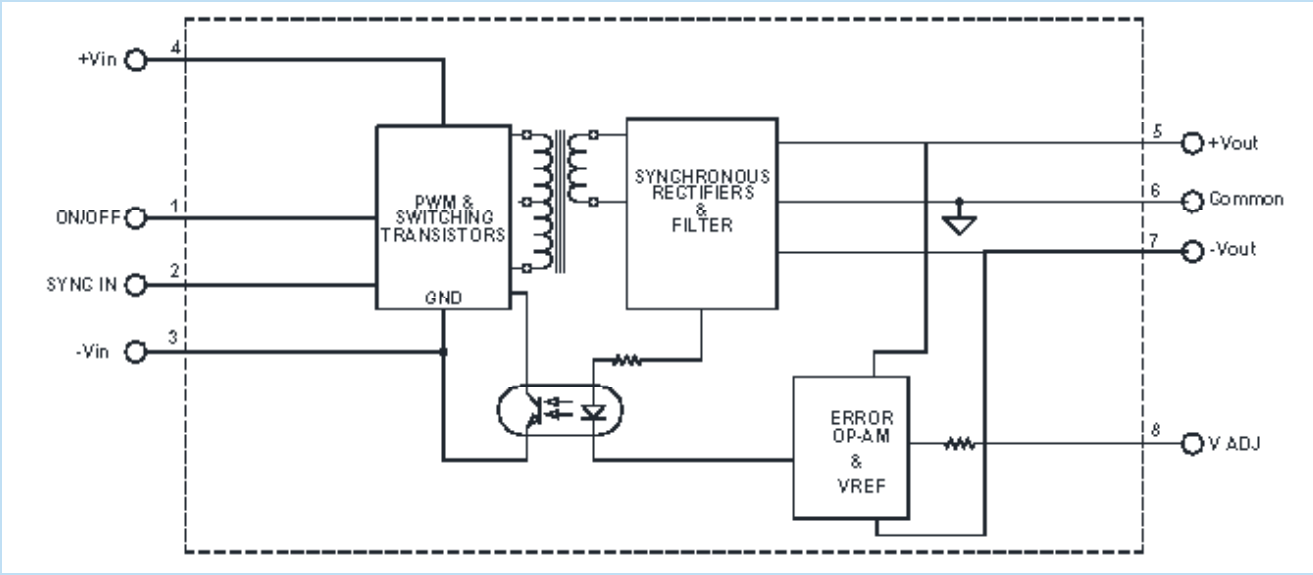
Instrumentation

Test & Measurement

Telecom

Functional Description

The BHE30001 series is a high-performance, low-noise, isolated DC/DC converters consisting of dual output model. The converter will synchronize to an external clock frequency of >=300KHz. The converter also incorporates low switching noise techniques at its input and output to provide 6W of output power at 84% efficiency in a 1.98x1.58x.40 case. It's high efficiency and SMT Technology allow the converter to operate from -40'C to +75'C without derating. All models are designed to meet the BASIC requirements of UL/EN60950-1 and CE mark.



Typical Block Diagram of BHE30001 Converter

Electrical Specifications

Unless otherwise specified, all parameters are given under typical +25°C with nominal input voltage and under full output load conditions.

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range		9	24	36	V
Input Current	Under Full Output Load(I_{OUT}=±500mA)		.282		A
Input Filter	LC				
Reverse Polarity Input Current	External series-blocking diode			12	A
Input Surge Current (20µS Spike)				10	A
Short Circuit Current Limit			150		% I_{IN}
Undervoltage Shutdown		6.5			Vdc
Off State Current,			2.5		mA
Remote ON/OFF Control, Positive Logic	Standard on All Model Reference to -Vin				
Converter ON	Open (Open Collector)				
Converter OFF		-0.6	0	0.2	Vdc
Logic Input Reference	-Input				
Logic Compatibility	TTL Open Collector or CMOS Open Drain				
Synchronization	TTL/CMOS, 15µS minimum pulse, 300µS peroid				
	Synchronization Reference to -Vin				
	See Notes on External Synchronization				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Voltage Ratings			±5.7		Vdc
Current Ratings			±500		mA
Output Voltage Accuracy			±1	±1.5	%
Output Voltage Adjustment				±10	%
Ripple & Noise (20 MHz Bandwidth)	See Figure 2,3,4,5,8		1	1.5	% of V_{PP}
Line Regulation	Minimum V_{IN} to maximum V_{IN}		±.5	±1.0	%
Load Regulation	NL to FL		±.2	±.5	%
Temperature Coefficient @ FL			0.02		%/°C of V_{OUT}
Transient Response Time (to within 0.5% of V_{OUT})	50% FL to FL to 50% FL, See Figure 1		50		µS
Short Circuit Protection	All outputs, by Hiccup technique				
Output Current Limit			1		A

ENVIROMENTAL & GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency			84		%
Isolation Voltage (1 min.)			1500		Vdc
Isolation Resistance			100		MΩ
Isolation Capacitance			1090		pF
Switching Frequency			300		kHz
MTBF	per MIL-HNBK-217F(Ground Benign, +25C)		1 x 10^6		Hours
Operating Temperature, Industrial		-40		+75	°C/W
Maximum Operating Case Temperature				110	°C
EMI/RFI	Six-sided continuous shielded metal case				
Humidity	Up to 95% non-condensing				

PHYSICAL CHARACTERISTICS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (L×W×H)	1.98×1.58×0.400 in. (50.29×40.13×10.16mm)				
Weight	1.80 oz. (51.02g)				
Case Material	Coated metal				
Shielding Connection	-Input (Pin 3)				

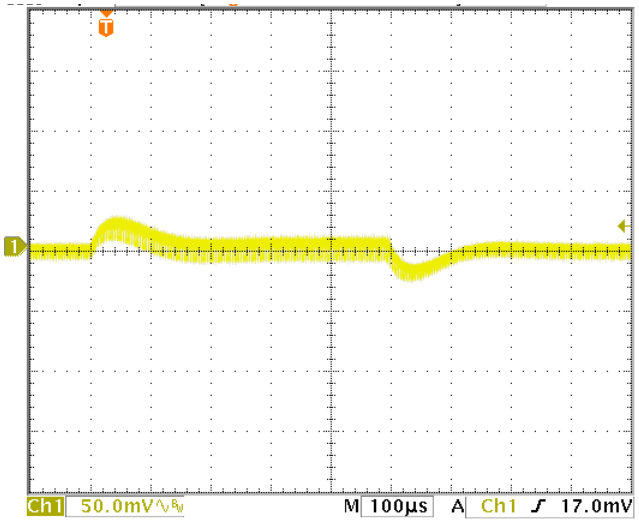


FIGURE 1. Transient response of BHE30001 from Full load to Half Load .

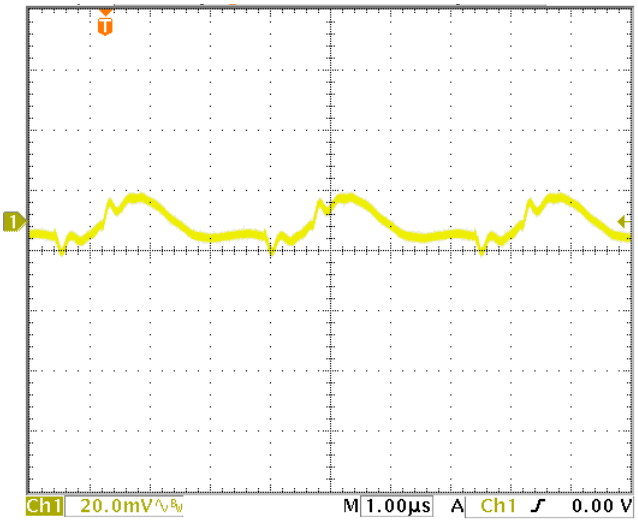


FIGURE 2. Typical output ripple of $+V_{OUT}$ ripple at V_{IN}=24V, I_{OUT}=0.5A as shown in Figure 8.

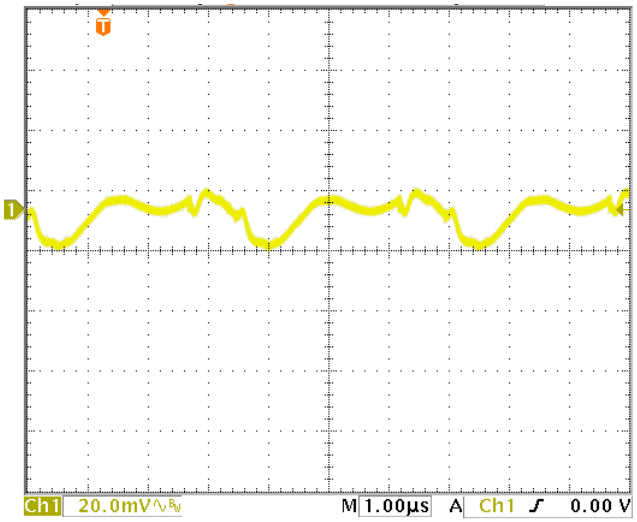


FIGURE 3. Typical output ripple of $-V_{OUT}$ ripple at V_{IN}= 24V, I_{OUT}= -0.5A as shown in Figure 8.

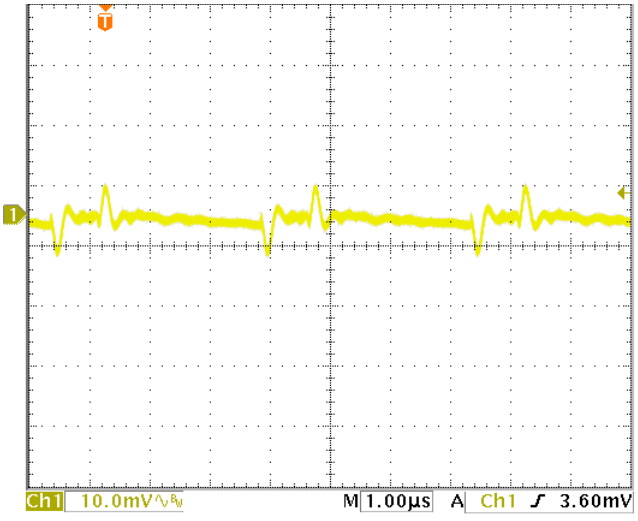


FIGURE 4. Typical output ripple of $+V_{OUT}$ ripple at V_{IN}=24V, I_{OUT}=0.5A as shown in Figure 8 with an additional 180uF@16V low esr cap.

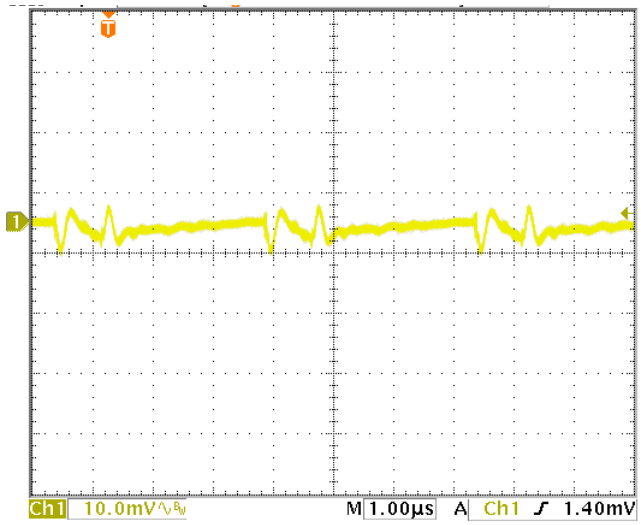


FIGURE 5. Typical output ripple of $-V_{OUT}$ ripple at V_{IN}=24V, I_{OUT}=-0.5A as shown in Figure 8 with an additional 180uF@16V low esr cap.

EXTERNAL SYNCHRONIZATION

The SYNC pin can be used to synchronize the internal oscilllator to external clock. An open drain output is the recommended interface between the external clock to the BHE30001 SYNC pin as shown in figure 6. The clock pulse width must be greater than 15ns. The external clock frequency must be greater than the frequency of the BHE30001.

Multiple BHE30001 converters can be synchronized together simply by connecting the converters SYNC pins together as shown in figure 7.

Care should be taken to ensure the ground potential differences between the converters are minimized. In this configuration all the converters will be synchronized to the highest frequeny device. The SYNC pin is a CMOS buffer with pull-up current limited to 200micro amps. If the external device forces the SYNC pin low before the internal oscillator ramp completes its charging cycle, the ramp will reset and another cycle begins. If the SYNC pins of multiple BHE30001 converters are connected together, the first SYNC pin that pulls low will reset the oscillator ramp of all the other converters. All converters will operate in phase when synchronized using the SYNC feature. Up to five devices can be synchronized using this method.

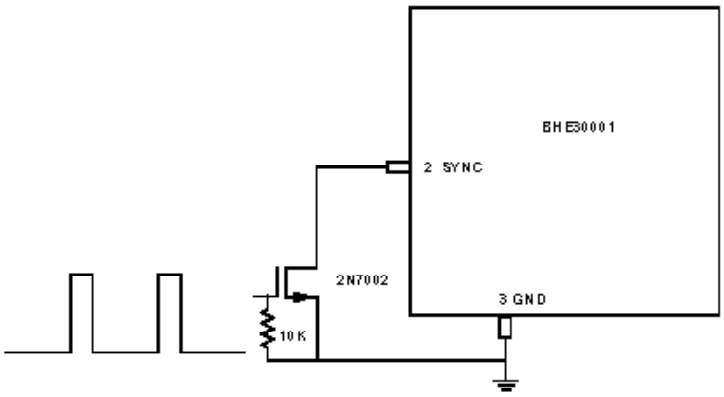


FIGURE 6. SYNC from external clock

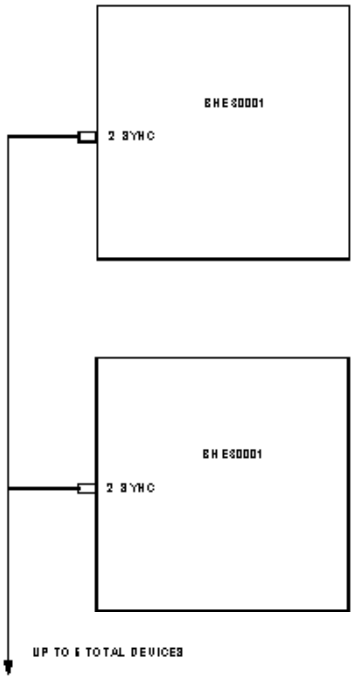
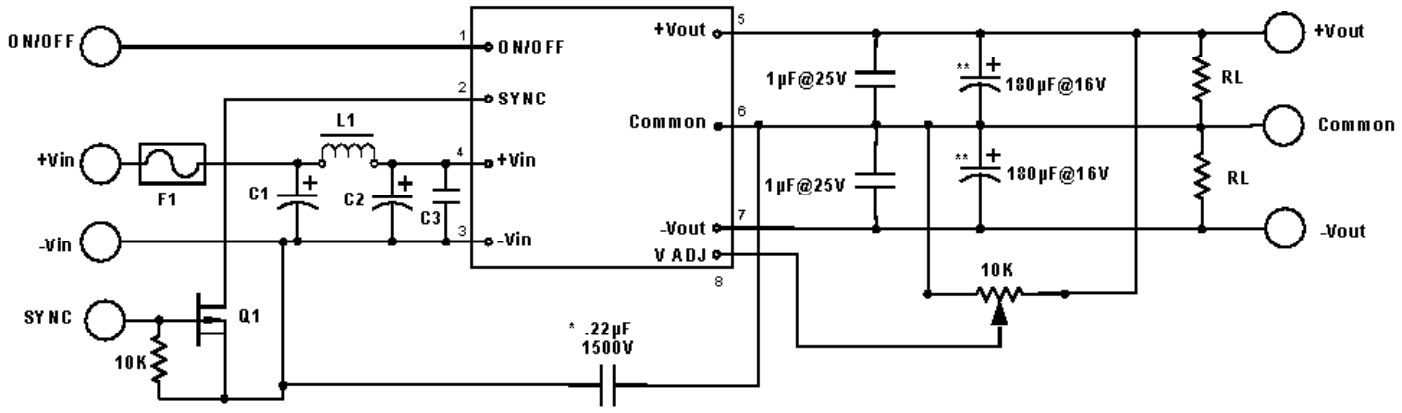


FIGURE 7. SYNC of multiple devices



** OPTIONAL PART TO FURTHER REDUCE OUTPUT RIPPLE

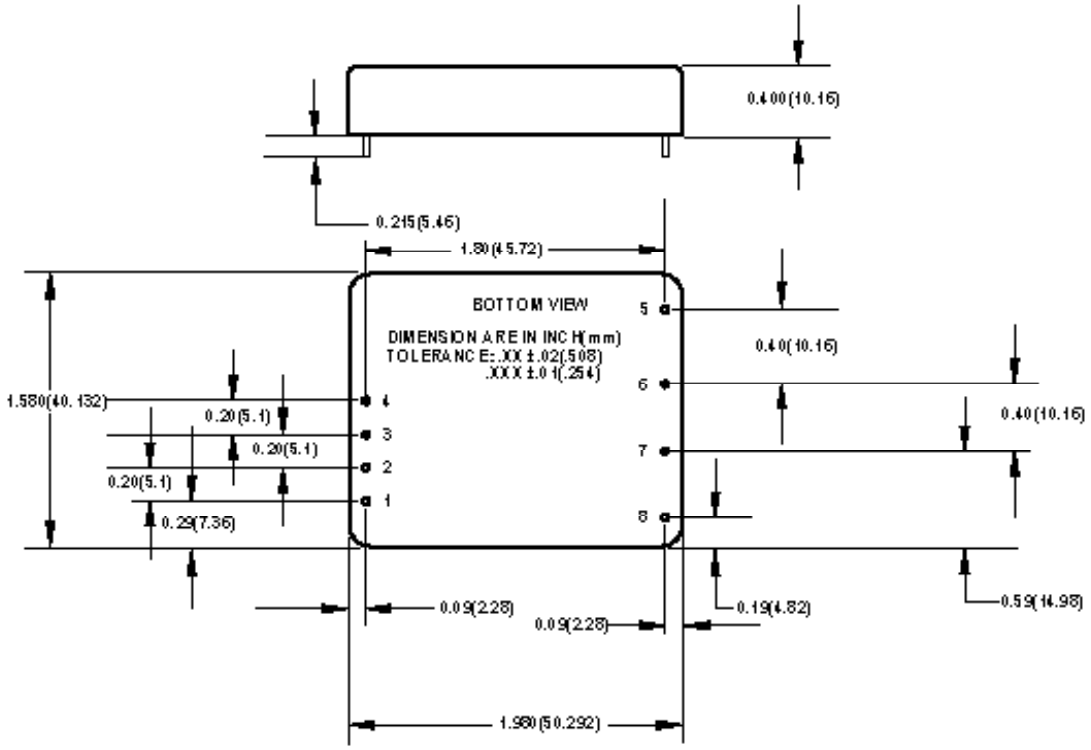
* OPTIONAL PARTS

Q1 = 2N7002 OR EQUIVALENT

V_{IN}	F1 (A)	C1/C2 (µF)	L1 (µH)	C3 (µF) ceramic
24	1	47@100V	1	2.2@100V

FIGURE 8. Typical connection diagram of BHE30001 DC/DC Converter

MECHANICAL SPECIFICATIONS



Pin	Function
	SINGLE
1	ON/OFF
2	SYNC
3	$-V_{IN}$
4	$+V_{IN}$
5	$+V_{OUT}$
6	Common
7	$-V_{OUT}$
8	V_{OUT} ADJ