PowerWatt ™

75W SINGLE DC/DC CONVERTER

2.3”×1”×0.4” - Smaller than Quarter Brick

Patented Technology

Key Features

- Efficiency up to 93%
- Power density of 98W/in^3
- 100µS transient response time
- 500µA off state current
- Output synchronous rectification
- 2:1 input voltage range
- Input-to-output isolation
- Soft start
- Short circuit protection
- Thermal protection
- Undervoltage protection
- External synchronization (Optional)

Beta Dyne is protected under various patents, including but not limited to U.S. Patent numbers: 5,777,519; 6,188,276; 6,262,901; 6,452,818; 6,473,3171.

Applications

Electronic Data Processing (EDP)

Instrumentation/Industrial/Medical

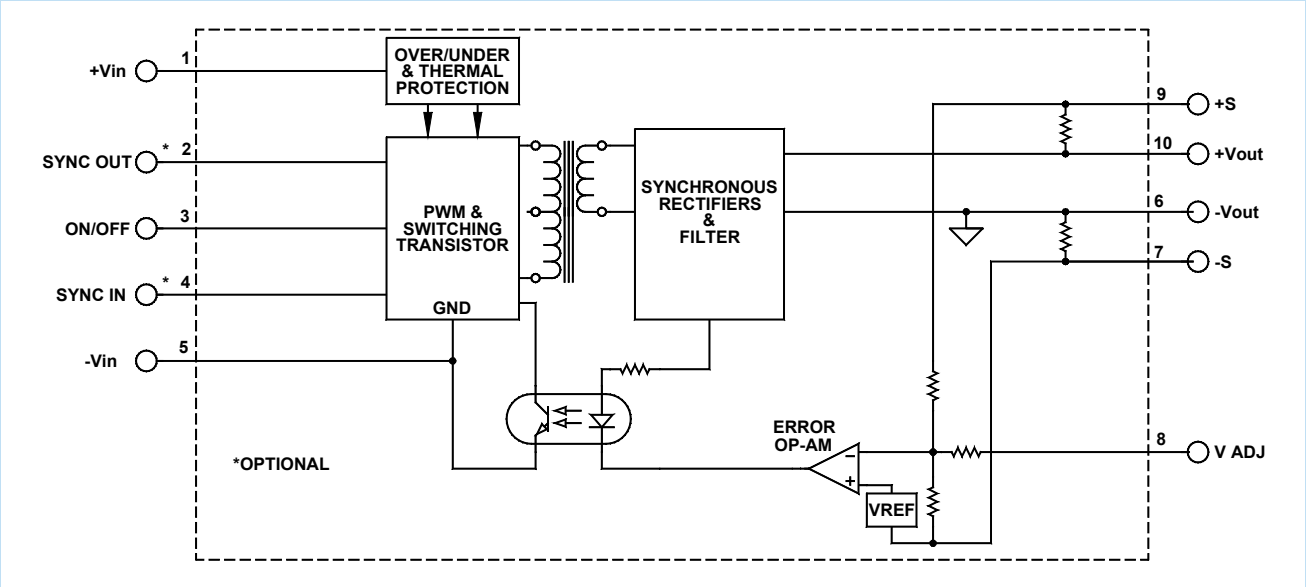
Communications

Computers

Fiber Optics

Functional Description

The 75W series is a family of single-output DC/DC converters in a through-hole 2.3×1×0.4-inch package. Their high efficiency and power density is a result of innovative patented designs utilizing improved synchronous rectification techniques and planar magnetics. The high efficiency, coupled with a multilayer PCB and thermal management, minimizes power dissipation and allow the converters to operate without an external heatsink. **If a heatsink is required, please see our Q75 75W DC/DC Converter series.**



Typical Block Diagram

Unless otherwise specified, all parameters are given under typical ambient temperature of +25°C with an airflow rate = 400LFM. With the given power derating, the operating range is -40°C to +125°C. Specifications subject to change without notice.

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

PARAMETER / VALUE / UNIT	PARAMETER / VALUE / UNIT
Input Voltage Non-operating..... 75Vdc continuous Operating..... 75Vdc contnuous Input/Output Isolation..... 1500Vdc Operating Temperature..... -40 to +125°C Storage Temperature..... -55 to +125°C	Voltage at On/Off Input Pin..... +40/-1Vdc Semiconductor Junction Temperature..... 150°C PCB Operating Temperature..... 150°C Pins Current Rating..... 30A@25°C Output Capacitance..... 20,000µF

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range	See Model Selection Guide				
Input Startup Voltage, 48V_{IN}				35	Vdc
Input Startup Voltage, 24V_{IN}				16.5	Vdc
Undervoltage Shutdown, 48V_{IN}		32			Vdc
Undervoltage Shutdown, 24V_{IN}		16			Vdc
Input Filter	Capacitor				
Reflected Ripple	See Model Selection Guide, Figure 1				mA_{PP}
No Load Input Current	See Model Selection Guide				
Input Surge Current (20µS Spike)				10	A
Short Circuit Current Limit			125	150	% I_{IN} Max
Off State Current			150		µA
Remote ON/OFF Control					
Supply ON	Pin 5 Open (Open circuit voltage: 12V Max.)				
Supply OFF		0		0.8	Vdc
Logic Input Reference					
Logic Compatibility	TTL Open Collector or CMOS Open Drain				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Voltage and Current Ratings	See Model Selection Guide				
Output Voltage Accuracy			±1		%
Output Voltage Adjustment	See also footnote 3 in Model Selection Guide		±5		%
Output Capacitance, V_O5V		470	1000	20000	µF
Output Capacitance, V_O18V		100	220	1000	µF
Ripple & Noise	Case must be grounded, see page 13.		1	2	%V_{PP} of V_{OUT}
Line Regulation	Minimum V_{IN} to maximum V_{IN}		±0.25	±0.5	%
Load Regulation	10% FL to FL		±0.25	±0.5	%
Output Minimum Load		5	10		%
Temperature Coefficient @ FL			0.02		%/°C
Transient Response Time	50% FL to FL to 50% FL, See Figure 3		50	100	µS
Short Circuit Protection	By input current limiting				
Turn On Delay with Soft Start	See Figure 4		3	4	mS
Output Overvoltage Protection	None,				

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency (at full power)	See Model Selection Guide and Figures 2 & 5				
Isolation Voltage (1 min.), Input to Output	All models		1500		Vdc
Isolation Resistance			10^9		Ω
Isolation Capacitance			300		pF
Switching Frequency		360	380	400	kHz

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Operating Temperature Range (Ambient)	Industrial, See Figures 9 & 10	-40		+71	°C
Storage Temperature Range		-55		+150	°C
Maximum Operating PCB Temperature	Case must be grounded, see page 13.			125	°C
Derating	See Figures 9 & 10				
Thermal Resistance[4]					
Open-frame (PCB Average Resistance)	Zero air flow		14		°C/W
With Heat Sink	Zero air flow		7.8		°C/W
Cooling	See Figures 9 & 10				
MTBF	per MIL-HNBK-217F (Ground benign, +25°C)		1.1×10^6		hours

PHYSICAL CHARACTERISTICS

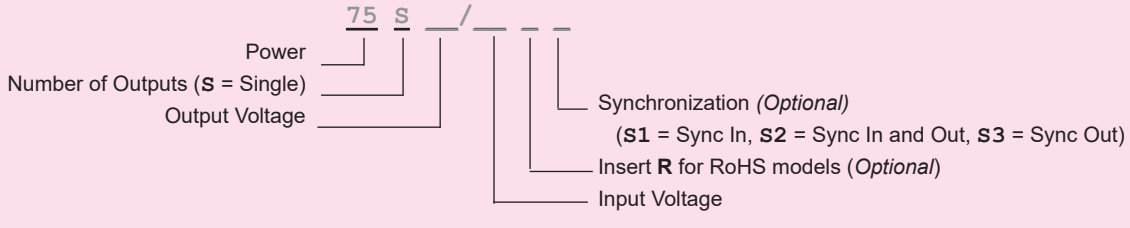
PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (L×W×H)	2.30×1.00×0.40 in. (58.42×25.40×10.16mm)				
Weight	1.1 oz. (31g)				

Model Selection Guide

MODEL NUMBER	INPUT					OUTPUT			
	Voltage (Vdc)		Current (mA)		Reflected Ripple[2] (mA_{PP})	Voltage (Vdc)	Current (A)	Efficiency (%)	
	Nominal	Range	No Load	Full Load[1]				50% FL	100% FL
75S1.8/24[3]	24	18–36	80	1786	80	1.8	20	86	84
75S2.5/24	24	18–36	80	2422	80	2.5	20	88	86
75S3.3/24	24	18–36	80	3230	80	3.3	20	90	86
75S5/24	24	18–36	80	3511	80	5.0	15	91	89
75S10/24	24	18–36	130	2940	80	10	6	87	85
75S12/24	24	18–36	80	2874	80	12	5	90	87
75S15/24	24	18–36	80	2841	80	15	4	90	88
75S18/24	24	18–36	80	3450	80	18	4	92	87
75S24/24	24	18–36	240	3550	80	24	3.125	90	88
75S1.8/48[3]	48	36–72	40	8823	40	1.8	20	88	85
75S2.5/48	48	36–72	40	1197	40	2.5	20	90	87
75S3.3/48	48	36–72	40	1559	40	3.3	20	92	89
75S5/48	48	36–72	40	1736	40	5.0	15	93	90
75S10/48	48	36–72	40	1453	40	10	6	88	86
75S12/48	48	36–72	40	1705	40	12	6	91	88
75S15/48	48	36–72	60	1736	40	15	5	91	90
75S18/48	48	36–72	40	2106	40	18	5	91	89
75S24/48	48	36–72	40	1736	40	24	3.125	92	90

[1] The maximum input current at any given input range measured at minimum input voltage is given as $1.6*I_{NOMINAL}$. Nominal input current is the typical value measured at the input of the converter under full-load room temperature and nominal input voltage (24Vdc and 48Vdc).
[2] Measured with 22µF capacitor for $48V_{IN}$ and 100µF capacitor for $24V_{IN}$ at the input power pins in series with 10µH inductor (see Figure 1A).
[3] The $1.8V_{OUT}$ models have ±20% output voltage adjustment range from $1.5V_{OUT}$ to $2V_{OUT}$.
[4] See Application Note DC-004: Thermal Considerations for DC/DC Converters.

ORDERING GUIDE



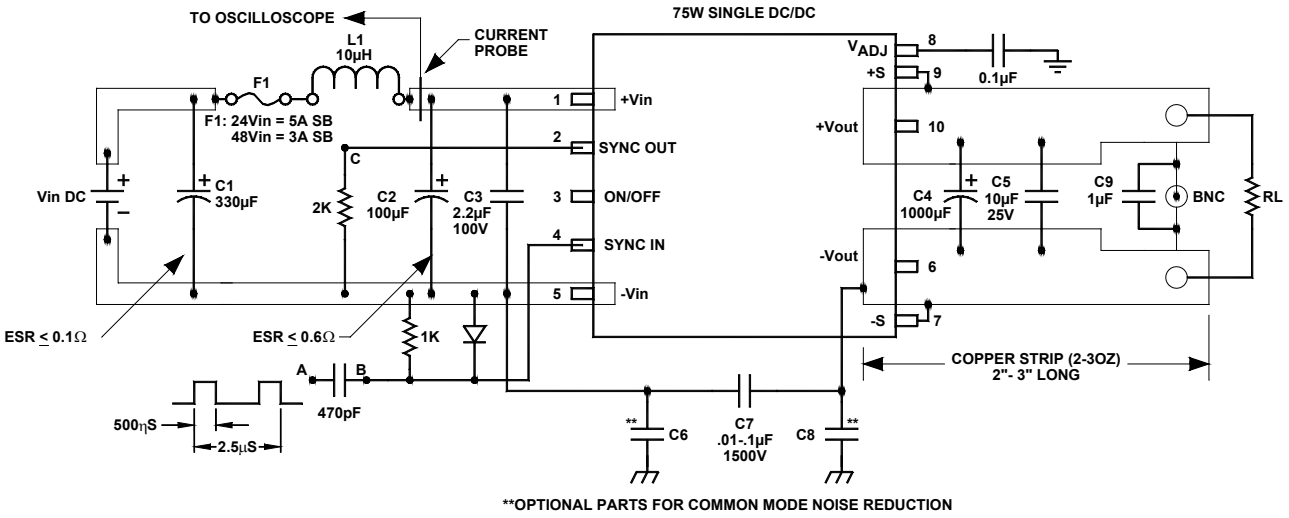


FIGURE 1A. Setup for output and reflected ripple measurement

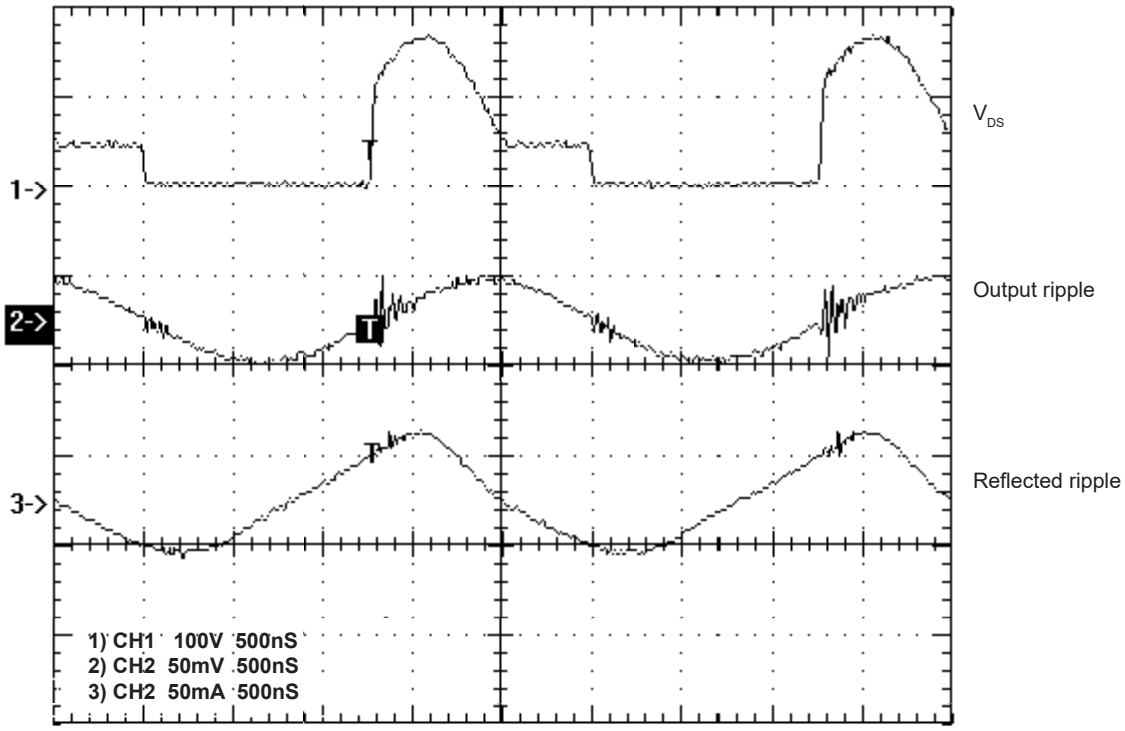


FIGURE 1B. Typical output ripple and reflected ripple of 75S5/48 (C_4 = 1000µF)

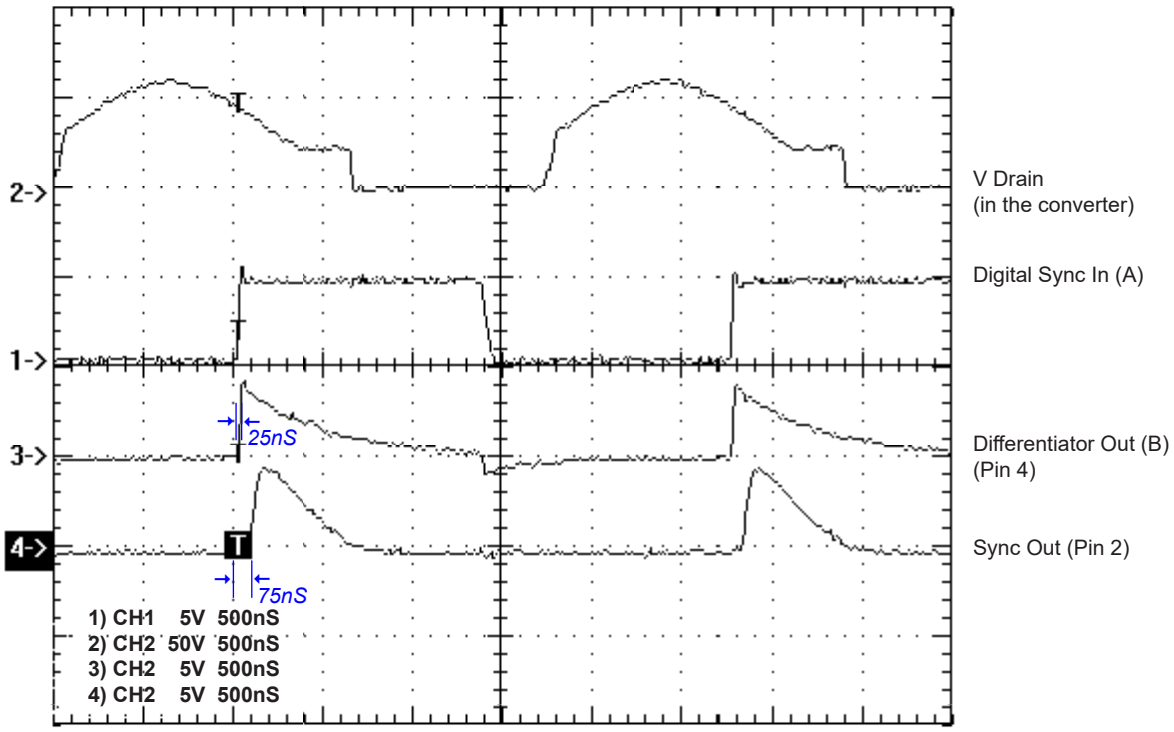


FIGURE 1C. Typical synchronization waveforms obtained from connection diagram in Figure 1 (75S3.3/24)

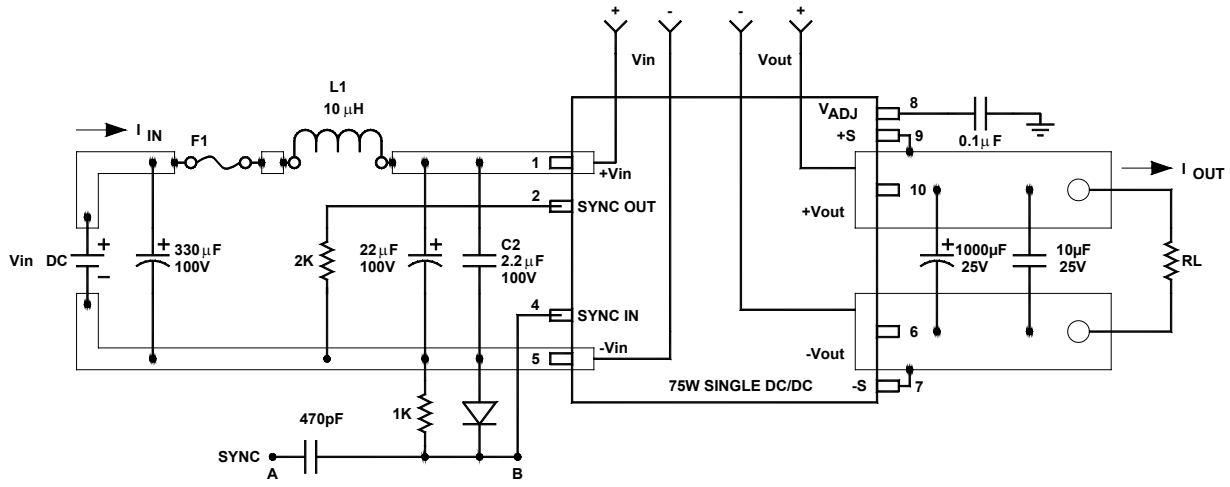


FIGURE 2. Setup for efficiency measurements

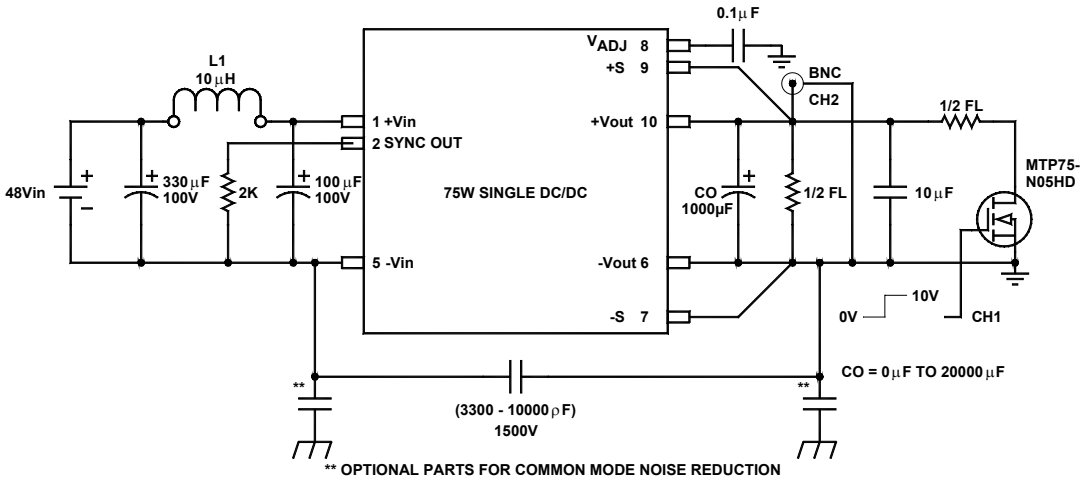


FIGURE 3A. Setup for transient response measurements

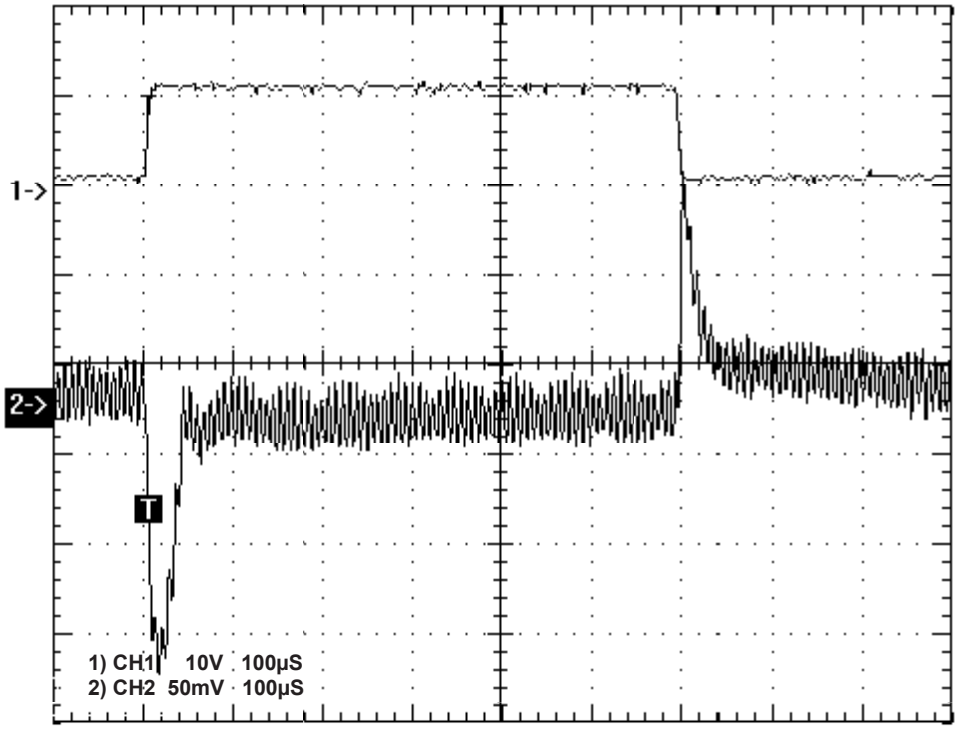


FIGURE 3B. Typical transient response of 75S3.3/48 (C_O = 1000µF, I_O = 50% FL to FL)

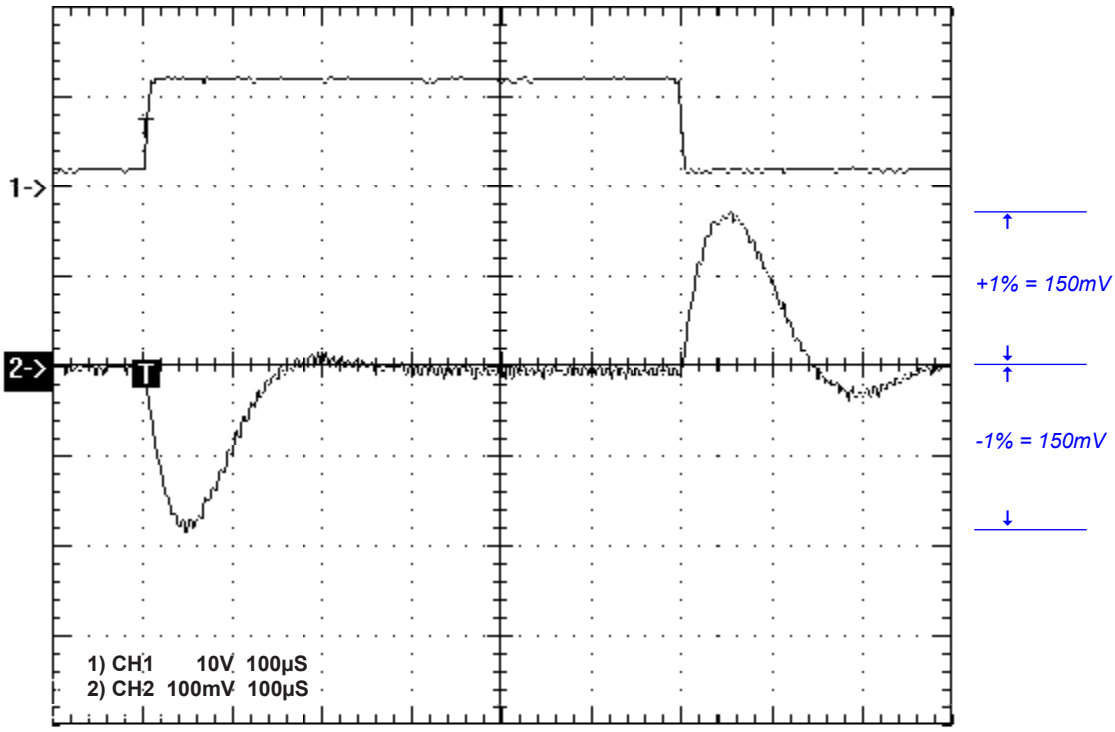


FIGURE 3C. Typical transient response of 75S15/24
(C_O = 250µF, 50% I_O = 2A)

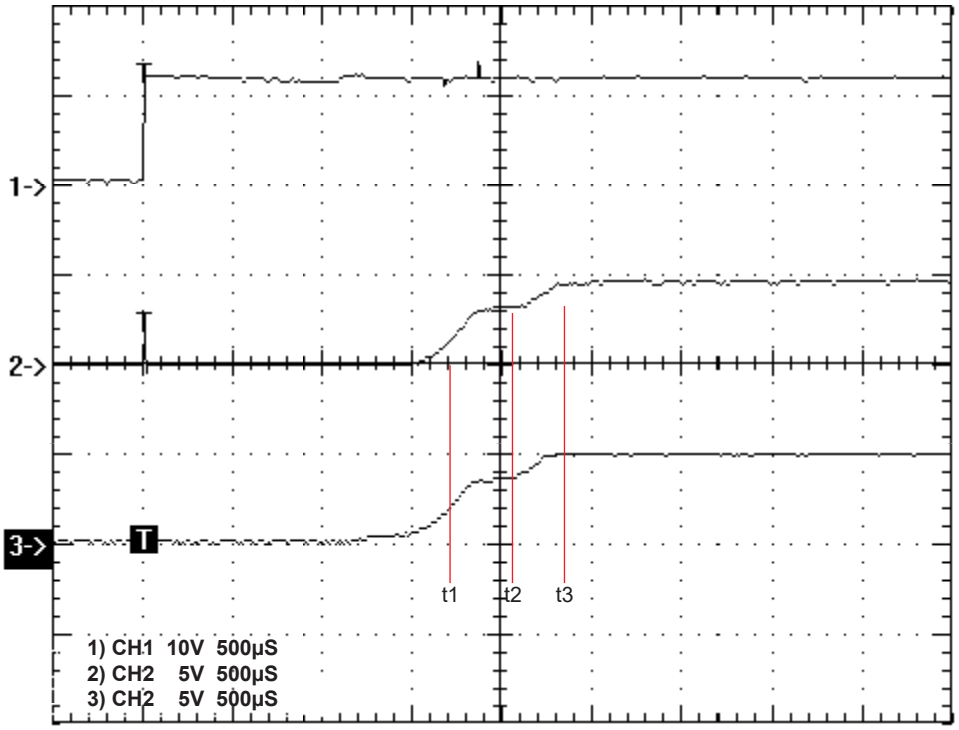


FIGURE 4. Turn on delays
(Refer to Figure 3A)

NOTE: From t1 to t2, the secondary voltage is rectified by the MOSFET parasitic diodes. From t2 to t3, a switchover from diode rectification to synchronous rectification occurs.

EXTERNAL TRIMMING OF OUTPUT VOLTAGES

To trim the output voltage DOWN, connect a 5% ¼W resistor between the + (plus) output and trim pin of the converter. To trim the output voltage UP, connect a 5% ¼W resistor between the – (minus) output and trim pins of the converter. For UP/DOWN trimming capability, connect a 10kΩ potentiometer between the + and – output pins, with the wiper arm connected to the trim pin.

The trim resistors/potentiometer can be connected at the converter output pins or the load. However, if connected at the load, the resistance of the runs becomes part of the feedback network which improves load regulation. If the load is some distance from the converter, the use of #20 gauge wire is recommended to avoid excessive voltage drop due to the resistance of the circuit paths.

See our application notes:
DC-001: Testing Transient Response in DC/DC Converters
DC-004: Thermal Consideration for DC/DC Converters

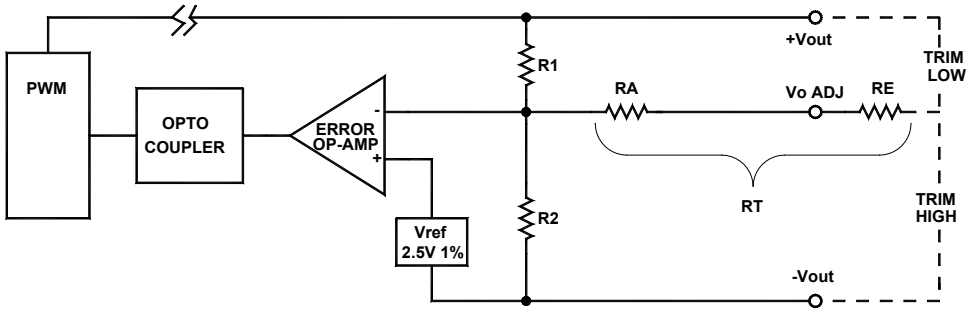


FIGURE 5. Output control circuit of 75W PowerWatt series

TABLE A. Output control components and references

V_O (V)	R1 (k)	R2 (k)	RA (k)	V_{REF} (V)
1.8	1.13	2.54	2.0	1.25
2.5	2.55	2.54	10.0	1.25
3.3	0.825	2.54	15.0	2.50
5	2.55	2.54	12.0	2.50
10	7.50	2.49	30.1	2.50
12	9.53	2.49	30.1	2.50
15	12.40	2.49	30.1	2.50
18	15.40	2.49	30.1	2.50

To trim V_O higher to V_O', where V_O is the actual measured untrimmed value:

$$RE = RT - RA = \frac{R1*V_{REF}}{V_O' - V_O} - RA$$

To trim V_O lower to V_O'', where V_O is the actual measured untrimmed value:

$$RE = RT - RA = \left[\left(\frac{R_1^2 * V_{REF}}{R_2(V_O - V_O'')} - R1 \right) - RA \right]$$

EXAMPLE

To trim V_O from 1.8V to 2V:

V_O = 1.8V, V_O' = 2V, R1 = 1.13kΩ, V_{REF} = 1.25, RA = 2kΩ

$$RE = RT - RA = \frac{1.13*1.25}{2-1.8} - 2k\Omega = 5.06k\Omega$$ *or* approx. 5.1kΩ (a standard resistor value)

EXTERNAL SYNCHRONIZATION

A TTL signal applied at the SYNC pin of the converter will synchronize the switching frequency of the converter to that of the TTL input signal. The external (TTL) frequency must be equal or higher than the converter's frequency. At the positive-going edge of the applied pulse, the internal power-switching transistor turns off and the PWM discharges its timing capacitor. At the negative-going edge, the PWM resumes normal operation. The minimum positive pulse width of the TTL signal must be 300nS and its frequency between 350kHz and 410kHz.

NOTE: Higher frequencies will reduce the efficiency of the converter and wide TTL pulses will force the PWM to follow the external TTL width modulation, which may effect regulation. A high TTL signal at the SYNC pin of the converter will turn the converter off. An internal pull-down resistor will keep this pin low when it is not used. A pulse differentiator (see Figure 7) can be used to shape a square wave sync signal as shown in Figure 6.

To avoid noise pickup, install a 1kΩ resistor from the SYNC IN (Pin 4) to $-V_{IN}$ (Pin 5). An internal current source will provide 2.5mA of current for driving another 75W converter from the SYNC OUT (Pin 2).

Please note that when the SYNC OUT pin is used to drive multiple converters, the 1kΩ sync input resistor is not required. However, a 2kΩ resistor load must be installed at the SYNC OUT pin (Pin 2) of the driving converter. The 2kΩ resistor can be the parallel combination of individual sync in resistors installed at the SYNC IN pin (Pin 4) of the converters to be driven.

For example, if a 75W converter "master" will be used to synchronize five other 75W converter "slaves," a 10kΩ resistor can be installed at the SYNC IN pin of each slave, and the SYNC OUT pin of the master can be connected to all the SYNC IN pins of the slaves.

The parallel combination of five 10kΩ resistors will provide the 2kΩ sync out load for the master. Avoid overloading the sync output current source with a resistor lower than 2kΩ. Overloading may affect the performance of the converter.

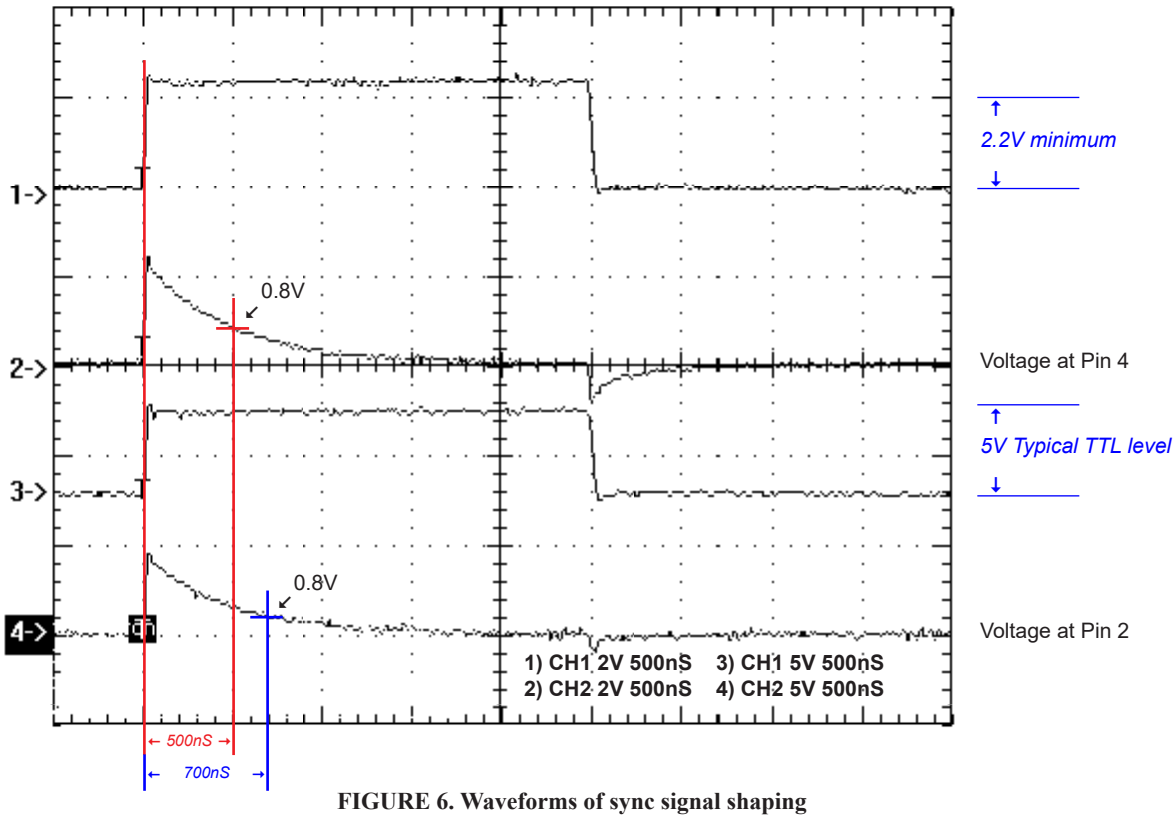


FIGURE 6. Waveforms of sync signal shaping

SYNC SIGNAL SHAPING

As described in External Synchronization, the PWM of the 75W converter requires a TTL signal of 0.8 to 2Vdc minimum amplitude and minimum duration of 300nS. When such a signal is not available (through one shot multivibrator or other pulse-shaping circuits) a C-R differentiator, such as the one in Figure 7, can be used to shape a square wave TTL signal. As is shown by the oscillogram in Figure 6, the positive edge of the sync pulse must be 2V minimum and the decaying exponential must reach the low er threshold of 0.8Vdc in 300nS minimum from the positive edge. The parallel diode with the resistor is a small signal switching diode or a Schottky signal diode with 0.3 to 0.5V forward drop, it is used to clamp the voltage at Pin 2@-0.5Vdc. For other logic levels (such as 2.5 and 3.3), adjust the RC time constant to obtain the required timing.

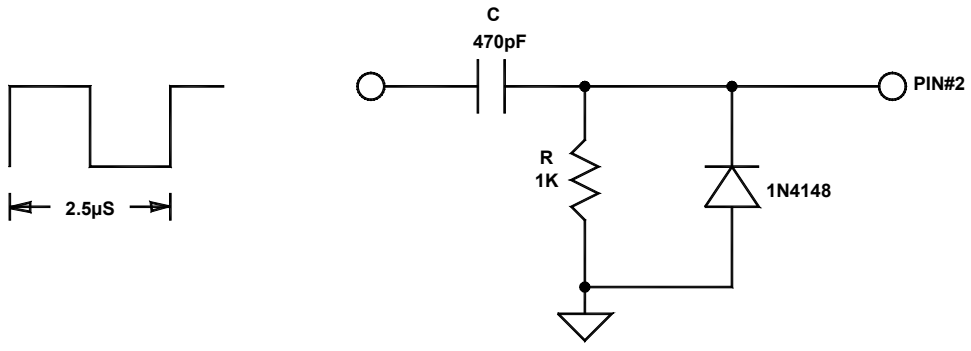


FIGURE 7. Suggested pulse-shaping circuit

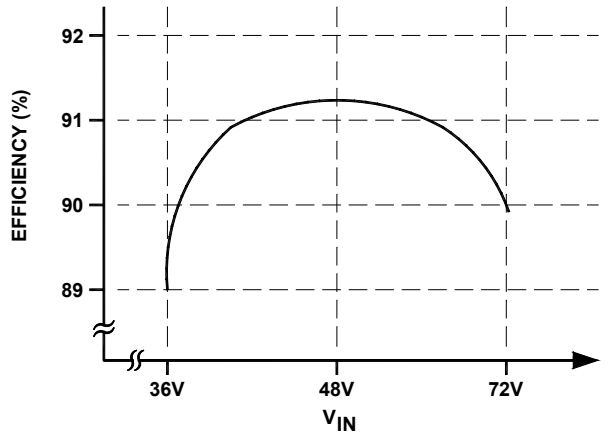


FIGURE 8A. Typical Efficiency vs. Input Line for $3.3V_{OUT}/48V_{IN}$

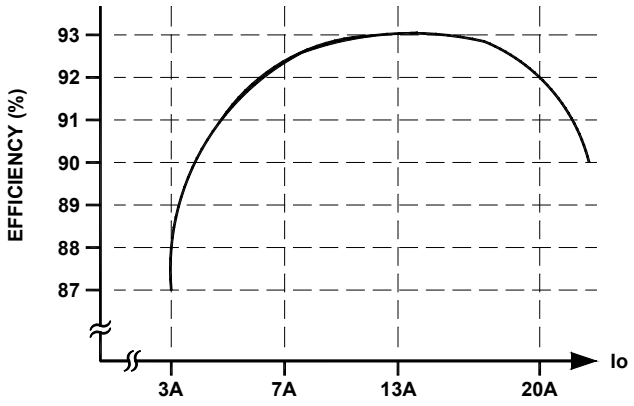


FIGURE 8B. Typical Efficiency vs. Load for $3.3V_{OUT}/48V_{IN}$

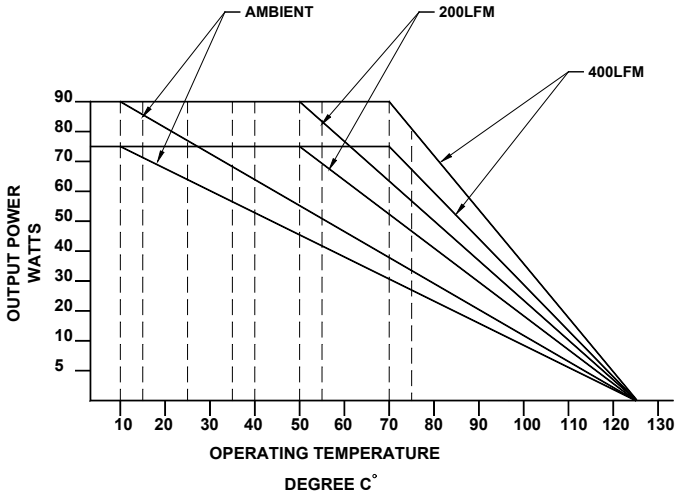


FIGURE 9A. Typical derating curves for 75W PowerWatt series without heat sink (For output power from 75W to 90W)

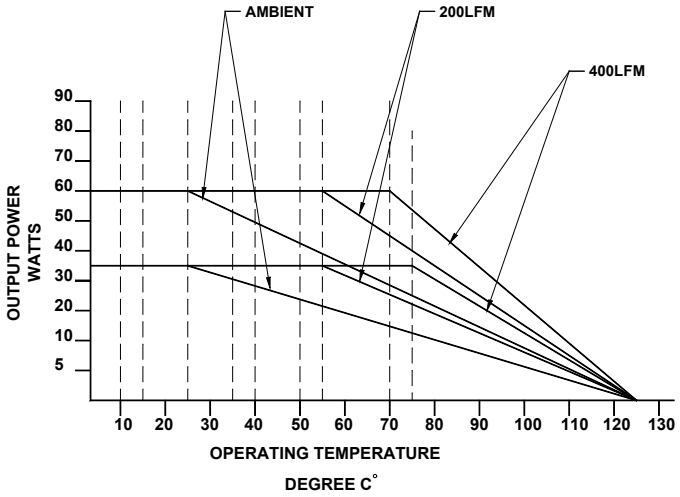
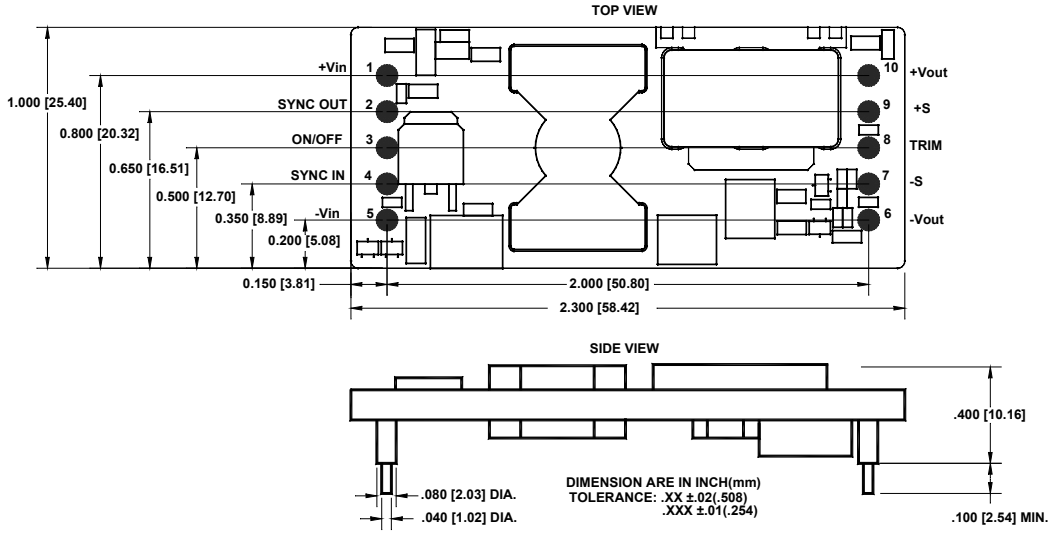


FIGURE 9B. Typical derating curves for 75W PowerWatt series without heat sink (For output power of 60W or less)

MECHANICAL SPECIFICATIONS



Pin	Function
1	$+V_{IN}$
2	SYNC OUT*
3	ON/OFF
4	SYNC IN*
5	$-V_{IN}$
6	$-V_{OUT}$
7	-S
8	TRIM
9	+S
10	$+V_{OUT}$

* Optional pins, See Ordering Guide

APPLICATION CONSIDERATIONS

Pin Functions

+V_{IN} (Pin 1): For positive input power supply connections.

SYNC OUT (Pin 2): Output-driving signal of the PWM.

ON/OFF (Pin 3): Turns converter off when pulled to ground through an open collector or open drain transistor. Maximum voltage at this pin is 12V minus a diode drop. Can be parallel connected with the ON/OFF pins of multiple converters or any Beta Dyne converter that may reside in the system. Leave this pin open for continuous operation.

SYNC IN (Pin 4): Input synchronization signal to the PWM. Used to synchronize the converter to an external frequency source.

-V_{IN} (Pin 5): For negative input power supply connection (or input ground).

-V_{OUT} (Pin 6): Negative output (GND).

-S (Pin 7): Negative output voltage sense; to be connected to the negative output at the load only.

V_{ADJ} (Pin 8): Output voltage adjust; to be used for an output voltage adjustment. Bypass this pin with a 0.01µF to 0.10µF capacitor.

+S (Pin 9): Positive output voltage sense; to be connected to the positive output voltage at the load only.

DESIGN CONSIDERATIONS

Input Source Impedance

The input of the converter should be connected to a low AC-impedance source. To reduce the impedance of a potentially high-inductive DC source, use a low ESR electrolytic capacitor (ESR < 0.6W@400kHz) mounted as close to the input pins as possible to ensure stability of the converter. As suggested in Figures 1 through 3, an electrolytic capacitor (22µF for 48V_{IN} or 47µF to 100µF for 24V_{IN}) in parallel with an SMD 2.2µF ceramic capacitor will ensure stability under any line or load condition. The 330µF capacitor before the input inductor L1 will reduce both reflected ripple and any long wire impedance from the DC source.

Output Filter Impedance

The impedance of an output filter may also affect the stability of a converter when additional low-pass filters are used. If additional output ripple reduction is required, avoid installing series inductors at the output. Instead, try to maximize output capacitance. The inductor of the output copper strips and a 1000µF capacitor will be enough for most applications. Low ESR electrolytic or tantalum capacitors can be used for additional output ripple reduction in parallel with ceramic capacitors for high-frequency attenuation. We recommend Vishay Sprague 594D Solid Tantalum Chip Capacitors.

THERMAL CONSIDERATIONS

Under full load, the PowerWatt 75W converters dissipate between 6W to 10W of power (depending on the model). The generated heat is transferred to the ambient by air conduction. At room temperature without any air movement, the operating environment of the converter is higher than room temperature, 25°–50°C higher, due to the fact that air around the converter heats up.

To measure the actual operating environment of the converter in a still air environment, place a thermocoupler a half-inch above the top center of the converter. Perform the same temperature measurement in a forced air convection system and use those temperature values for your thermal calculations. Do not assume the temperature is constant throughout a forced air cooling system! Surrounding components and the load can cause the converter to go to thermal shutdown.

The minimum junction temperature of all semiconductors is 150°C and the maximum operating temperature of the PCB is 150°C. When the temperature of the PCB reaches approximately 125°C, the converter will turn off. The thermal hysterisis of 20°–30°C will allow the converter to cool off and resume operation once it reaches approximately 95°C. If there is not enough air circulation due to air fan failure of the system or very high environmental temperatures, the converter will stay in this so-called “hiccup” (ON/OFF) thermal mode indefinitely.

EFFICIENCY MEASUREMENTS

Using the setup given in Figure 2, measure the input and output voltage at the pins at the top of the multiplayer PCB and use these values to calculate the efficiency. The voltage drop at full load at the output (20A when measured from the top of the PCB to the other end of the pin) is 18mV at room temperature. Even though 18mV does not look bad, it accounts for approximately 0.4W of power dissipation for both the positive and negative output pins for a total power dissipation of 0.8W. A poor layout can cause this worst-case scenario; see ***Layout Considerations*** for more details.

SHORT CIRCUIT PROTECTION

The PowerWatt series of converters has a dual short circuit protection feature. At the input side of the converter, two short circuit current comparators are used to monitor the input current of the converter. They are biased at different voltage levels; the lower threshold (LTH) comparator provides the power limiting function of the converter. Under normal operating conditions, the LTH comparator limits the output power of the converter when the maximum output power is exceeded. When a hard short is applied across the output of the converter and the input current exceeds the set threshold of the second comparator, the converter goes into shutdown mode, the overcurrent latch is set and the converter is turned off. The converter will turn on again when its input voltage is recycled (OFF–ON) or if the ON/OFF pin is used to turn the converter on and off. The time required for the ON/OFF pin to be held low is between 100mS and 800mS.

LAYOUT CONSIDERATIONS

The maximum output current of the converter is 25A and is carried to the load through six 10A rated pins. When the converter is installed in a double-sided PCB, use both sides to connect the high current pins and use 2–3oz. copper for the plated through holes and/or power pads.

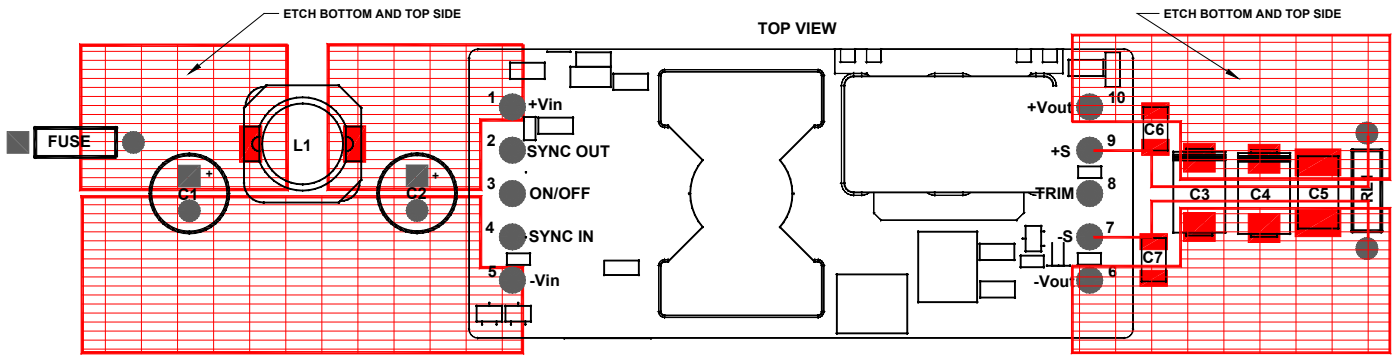
DO NOT USE sockets in production. For lab testing we recommend MILL-MAX sockets (P/N: 7406-0-15-01-18-01-04-0) or any other socket that offers a maximum conductive surface to the pins.

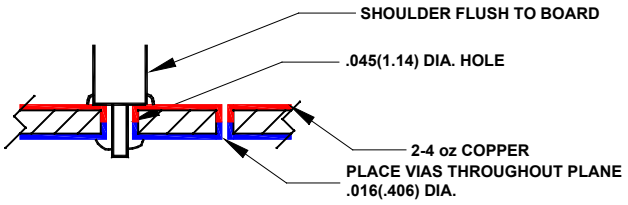
If possible, maximize the surface area on the board for the power pins and DO NOT install a solder mask (see Figure 10). A solder mask will trap the heat inside the PCB and will not allow for maximum heat transfer even in forced-air cooling systems.

To minimize any IR drop on the pins and reduce thermal resistance, the best solution is to place the multilayer PCB of the 50W on your PCB. The price you pay is a hole in your PCB. The IR drop from top to bottom at 20A is 1mV. The semiconductor junction temperature will drop by 30° to 50°C minimum in a 400LFM-cooled system (depending on the exposed area you allowed on the top and bottom surfaces of your PCB.)

Please note that in a multilayer PCB the inner layers do not contribute much in reducing the thermal resistance of the power component, they only reduce the resistance to the load. If the top and bottom layers of your PCB can be plated up to 3–4 oz., you do not have to use a multilayer PCB for the converter.

If the sense run length exceeds 2 inches, the sense pins may have to be bypassed at a point close to the converter. Keep in mind to bypass to their respective polarity. Avoid running digital signal lines parallel to the sense pins. If more than one power device or converter is used per system board, use a star ground connection





SUGGESTED PARTS

	24Vin	48Vin
FUSE	PICO II 4A@125V S.B.	PICO II 4A@125V S.B.
L1	10µH SUMIDA PT#CDRH104R-100	10µH SUMIDA PT#CDRH104R-100
C1&C2	47µF-100µF UNITED CHEMI-CON	22µF-47µF@100V UNITED CHEMI-CON
C3&C4	100µF - 470µF SPRAGUE	100µF - 470µF SPRAGUE
C5	10µF CERAMIC UNITED CHEMI-CON	10µF CERAMIC UNITED CHEMI-CON
C6 & C7	.01µF-.1µF CERAMIC	.01µF-.1µF CERAMIC

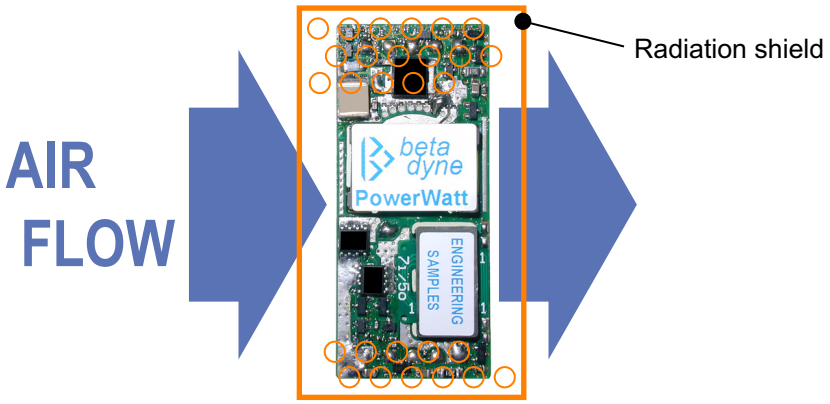
NOTES:
1. DIMENSIONS ARE IN INCH(mm).
2. TOLERANCE: .XXX ± .005

FIGURE 10. Suggested layout of 75W PowerWatt series

EMI/RFI IN OPEN-FRAME DC/DC CONVERTERS

All switching AC/DC and DC/DC converters generate noise due to high-voltage, high-current internal switching. Conducted noise is the noise that appears at the point of conduct (pins) of the converter. Radiated noise is the electromagnetic noise transmitted to the environment from the power source. Conducted noise can be reduced to acceptable levels by an input/output low-pass filter.

In the past, manufacturers used metal cases and conductive headers to provide six-sided shielding to prevent radiated noise. Open-frame converters, on the other hand, have no shield and all the high-voltage, high-current switching points radiate noise. Open-frame, high-density DC/DC converters use forced air cooling. Most of the switching transistors are placed at the top of the converter to allow for better air circulation. Also, these switching transistors and power magnetics will produce square current/voltage waveforms that are full of harmonics. Most open-frame converters use fixed switching frequencies from 200kHz to 1MHz. The high switching frequencies can generate harmonics from 1MHz up to several hundred MHz.



DRAWING A

Effective placement and orientation of the converter in a system with forced air cooling can reduce the case temperature by 5–15°C (depending on the air flow (LFM)). When the converter is placed at the entrance and air passes over it as shown in Drawing A—from Pin 5–1 and 6–10—the lowest case temperature can be obtained.

Therefore, open-frame converters require special consideration in three critical areas—layout, radiation and cooling—that may create conflicts. We stress the importance of these critical areas:

LAYOUT
RADIATION
COOLING

When an open-frame converter is used to power digital circuits, radiation shielding can be implemented via the system shielding. When the load is an analog circuit—for example, A/D, D/A, RF amplifier, etc.—and these components are placed close to the converter, the radiated noise may affect signal integrity.

High impedance summing points of operational amplifiers or other components with poor power supply rejection ratio (PSRR) may be affected. In this case, local radiation shielding around the converter is necessary.

The shield must allow the forced air to pass freely over the converter (see Drawings A, B & C). A metal screen can be considered. The holes in the screen must be less than the wavelength of the noise. If the converter is placed far from the load, make sure thick PCB runs are used (2–3 oz. copper is sufficient.)

When noise creates problems in a system, it is very difficult to identify the source of the problem. A poor layout with ground loop can not only create noise it can also affect the stability of the converter or randomly trigger an event. A common problem in high frequency and high power density DC/DC converters is the so-called “common-mode noise,” which is the noise generated from parasitic capacitors, leakage inductance, etc. in the converter.

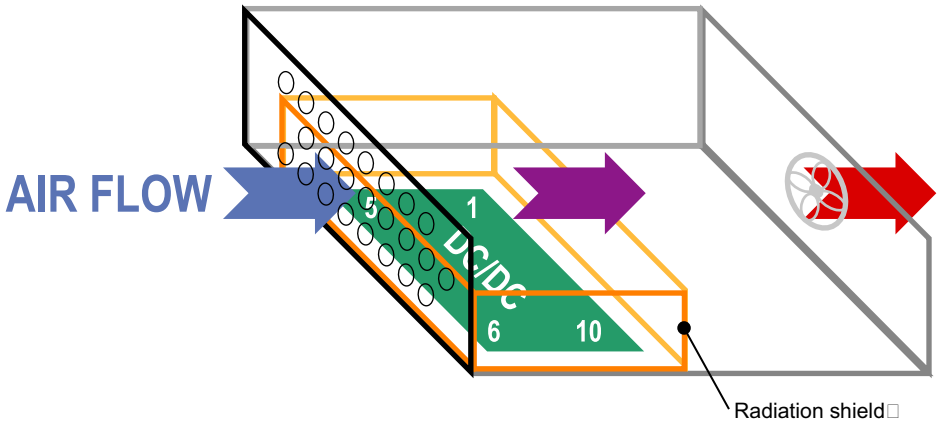
Common-mode noise (CMN) can be bypassed to chassis with small capacitors between input and output grounds to chassis and input and output ground. Assuming the layout is correct and the converter still generates noise, the question then becomes why does the system not exhibit a noise problem when a linear voltage source is supplied?

The answer comes from the process of elimination. Replacing a switching power source of 500kHz with another one switching at 50–60Hz is not the solution. Using the “noisy” DC/DC converter, one may try the following: First, if possible, shield the converter with six-sided shielding. If the problem is still in the system, then radiated noise is not the problem! Conducted noise or poor layout are the more likely causes. As was mentioned earlier, the use of a component with poor PSRR—e.g. BICMOS, CMOS, rail-to-rail OPAMS—may be the cause of the problem.

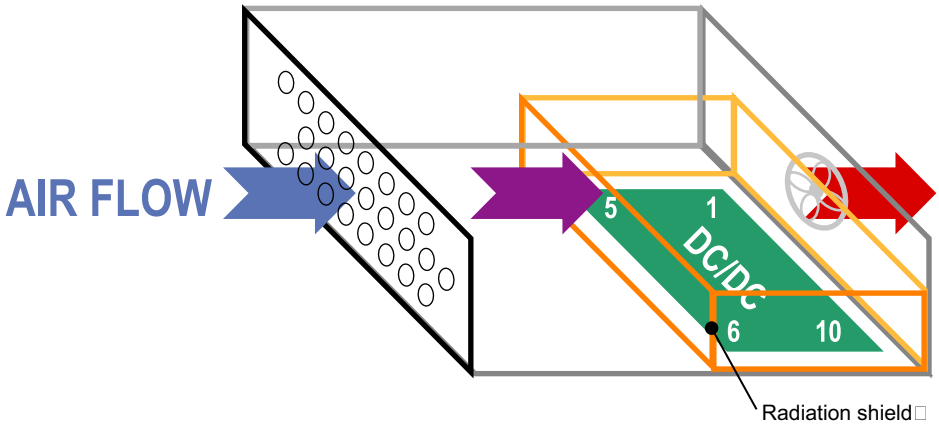
Do not use a converter with 50mV to 100mV output ripple to power a 12-bit A/D converter. Also keep in mind that CMOS, OPAMs, A/D, and S/H may offer low power, but the parasitic capacitor from drain to gate, drain to source, and gate to source will couple any V_{DD} and V_{SS} supply noise into your signal.

Better filtering in the input or output will reduce conducted noise if they are the cause of the problem. When both radiated and conducted noise are reduced, the last potential cause is ***layout***. Also, use ground plain under the converter for shielding and avoid passing signal lines under it.

In conclusion, open-frame DC/DC converters offer high efficiency, power density, and low cost, but radiate a wide band of noise. For any application where the system layout is critical, select the appropriate converter(s) for the application and completely test your system during the prototyping phase. DO NOT ASSUME all is well.



DRAWING B



DRAWING C