

30W DUAL DC/DC CONVERTER

3:1 Input Range, Dual Output
Parallel or Redundant Operation
~ Patent Pending ~

Key Features

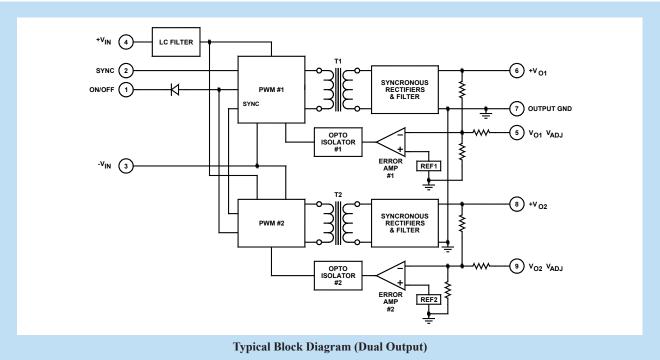
- · Wide input voltage range (3:1)
- Efficiency up to 85%
- Input-to-output isolation
- Input LC filter
- Soft start
- Short circuit protection
- 150µA off state current
- Multiple converter synchronization
- · Independently adjustable outputs
- Six-sided EMI shielding



Beta Dyne is protected under various patents, including but not limited to U.S. Patent numbers: 5,777,519; 6,188,276; 6,262,901; 6,452,818; 6,473,3171.

Functional Description

The 30W series is a family of dual 15W DC/DC converters that offer a wide 3:1 input voltage range, 400kHz switching frequency, forward topology and come packaged in a 2×2×0.395-inch case with an industry standard pinout arrangement. Synchronous rectification improves efficiency, while the dual independent control loop and independent output voltage adjustability, internal frequency synchronization, and load sharing/redundancy offer design flexibility. The six-sided shielding, SMD and improved thermal techniques enhance reliability.



Electrical Specifications INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range	See Model Selection Guide, Table 1				
Input Filter	LC				
Reverse Polarity	External series-blocking diode				
No Load Input Current	See Model Selection Guide				
Input Reflected Ripple	See Ordering Guide, Note 1				
Input Surge Current (20µS Spike)				10	Α
Short Circuit Current Limit				150	% I _{IN}
Undervoltage Shutdown			8		Vdc
Turn On Delay	Including Soft Start		4		mS
Off State Current				150	μΑ
Remote ON/OFF Control					
Supply ON	Pin 1 Open (Open circuit voltage: 12V Max.)				
Supply OFF		0		0.8	Vdc
Logic Input Reference	-Input				
Logic Compatibility	TTL Open Collector or CMOS Open Drain				
Converter Standby Input Current	See Model Selection Guide (No Load)				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Voltage and Current Ratings	See Model Selection Guide, Notes 2 & 3				
Output Voltage Accuracy			±1	±2	%
Output Voltage Adjustment	Per output	±3	±5		%
Ripple & Noise	(See App. Note DC-003)		75	100	mV _{PP}
Line Regulation			±0.5	±1	%
Load Regulation			±1		%
Temperature Coefficient @ FL			0.02		%/°C
Transient Response Time	50% FL to FL to 50% FL		100	150	μS
Short Circuit Protection	All outputs, by input current limiting				

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency (at full power)	See Model Selection Guide				
Isolation Voltage (1 min)			1500		Vdc
Isolation Resistance			10 ⁹		W
Isolation Capacitance			1000		pF
Switching Frequency			400		kHz

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Operating Temperature, Industrial (Ambient)		-40		+71	°C
Operating Temperature, Extended	Insert an x after model number (see Ordering Guide)	-55		+85	°C
Storage Temperature Range		-55		+125	°C
Thermal Resistance			5	6	°C/W _{DISS}
Derating	See Figure 1				
Humidity	Up to 95% non-condensing				
Cooling	Free-air convection				
EMI/RFI	Six-sided continuous shielded metal case				
MTBF	per MIL-HNBK-217F (Ground benign, +25°C)		700,000		hours

PHYSICAL CHARACTERISTICS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (L×W×H)	2.00×2.00×0.395 in. (50.80×50.80×10.03mm)				
Weight	2 oz. (58g)				
Case Material	Coated metal				
Shielding Connection, 24V _{IN}	-V _{IN} (Pin 3)				
Shielding Connection, 48V _{IN}	+V _{IN} (Pin 4)				

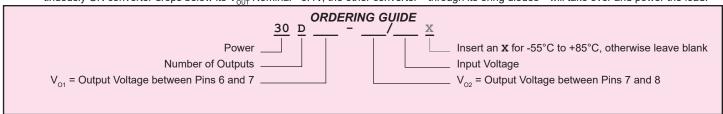
Model Selection Guide

MODEL NUMBER		INPUT			ОИТРИТ				
	Voltag	e (Vdc)	Currei	nt (mA)	Reflected Ripple (mA _{PP})	IVIAA	Voltage (Vdc)	Current (mA)	Efficiency Full Load (%)
	Nominal	Range	No Load	Full Load			(Vo1-Vo2)		
30D2.5-1.8/24	24	10–30	60	1220	10	3.80	2.5–1.8	5000/6000	79
30D3.3-1.8/24	24	10–30	60	1310	10	3.80	3.3–1.8	4500/6000	81
30D3.3-2.5/24	24	10–30	70	1370	10	3.80	3.3–2.5	4500/5000	81
30D5-1.8/24	24	10–30	70	1360	10	3.80	5.0-1.8	3000/6000	80
30D5-3.3/24	24	10–30	90	1480	10	3.80	5.0-3.3	3000/4500	83
30D12-5/24	24	10–30	60	1540	10	3.80	12–5	1250/3000	81
30D15-3.3/24	24	10–30	40	1520	10	3.80	15–3.3	1000/4500	81
30D2.5-1.8/48	48	20–60	40	600	5	1.90	2.5–1.8	5000/6000	81
30D3.3-1.8/48	48	20–60	40	650	5	1.90	3.3–1.8	4500/6000	83
30D3.3-2.5/48	48	20–60	40	690	5	1.90	3.3–2.5	4500/5000	83
30D3.3-3.3/48 *	48	20–60	40	740	5	1.90	3.3–3.3	9000	83
30D5-1.8/48	48	20–60	40	650	5	1.90	5.0-1.8	3000/6000	83
30D5-3.3/48	48	20–60	40	730	5	1.90	5.0-3.3	3000/4500	85
30D12-5/48	48	20–60	30	770	5	1.90	12–5	1250/3000	81
30D15-5/48	48	20–60	20	740	5	1.90	15–5	1000/3000	84
	С	ontact fact	ory for cus	tom input a	l Ind output volt	age co	mbinations		

For applications where more power is needed than that supplied by one of the outputs of the 30W series, both outputs of the 30W can be parallel connected. A parallel connection is possible provided that both outputs have the same nominal output voltage or through the V_{OUT} Adjust pins, in which both outputs can be adjusted for the same nominal V_{OUT} . For example, looking at the 30D2.5-1.8/48, where V_{O1} = 1.8V and V_{O2} = 2.5V, V_{O1} can be adjusted for higher output and V_{O2} can be adjusted for lower output. Assuming the required output is 2.2V and the total output current is 10A, the two individually adjusted outputs V_{O1} = V_{O2} = 2.2V can be parallel connected to share the output load. Both converters in the 30W family are internally synchronized and will NOT go to a hiccup protection mode, when their equal voltage outputs are connected in parallel. Careful layout, such as thick copper PCB runs from the pins to the load, star ground connection (to avoid ground loops) and filtering of input and control signals (as is shown below) will allow for equal current share and reliable system operation.

³ REDUNDANT OPERATION (Refer to Figure 4)

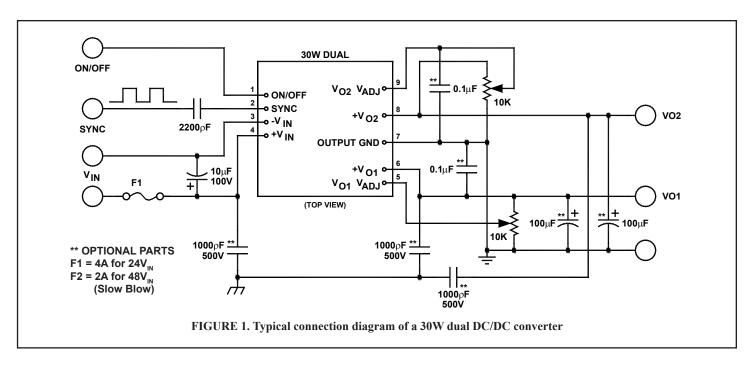
The 30W dual, equal-voltage output converter can be designed for redundant operation. In Figure 4, one of the outputs which is adjusted for Volta Nominal + 0.4V is ON and supplies all the power to the load while the other is OFF (standby). If for whatever reason the output voltage of the continuously ON converter drops below its V_{OUT} Nominal - 0.4V, the other converter—through its oring diodes—will take over and power the load.

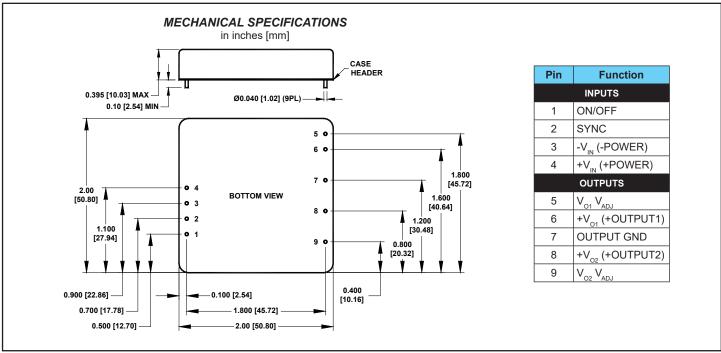


^{*} Parallel connect V_{01} and V_{02} for 9A I_{00T} .

1 Input reflected ripple is measured with a 100 μ F capacitor placed across the input power pins.

² PARALLEL OPERATION (Refer to Figure 3)





EXTERNAL SYNCHRONIZATION

The converter can be synchronized to an external TTL or CMOS clock signal. Insert a 470pF to 1000pF ceramic capacitor between the driving clock signal and the Sync pin (Pin 2) of the

convertor. The frequency of the signal must be between 370kHz to 450kHz and the duty cycle 20% high and 80% low. See application note DC-005: Synchronization.

EXTERNAL TRIMMING OF OUTPUT VOLTAGES

To trim the output voltage DOWN, connect a 5%, 1/4W resistor between the + (plus) output and trim pins of the converter. To trim the output voltage UP, connect a 5%, 1/4W resistor between the – (minus) output and trim pin of the converter. For UP/DOWN trimming capability, connect a $10k\Omega$ potentiometer between the + and – pins, with the wiper arm connected to the trim pin. The trim resistors/potentiometer can be connected at the converter output pins or the load. However, if connected at the load, the resistance of the runs becomes part of the feedback network, improving load BETA DYNE INC • www.betadynepower.com

regulation. If the load is some distance from the converter, the use of #20 gauge wire is recommended to avoid excessive voltage drop due to the resistance of the circuit paths.

See our application notes:

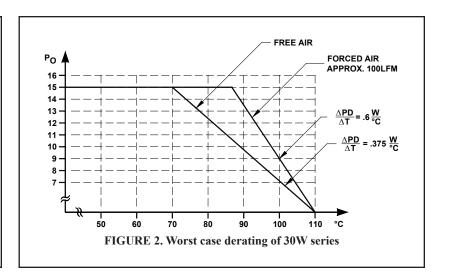
DC-001: Testing Transient Response in DC/DC Converters DC-004: Thermal Consideration for DC/DC Converters

DC-006: Synchronous Rectification

TABLE 1. Minimum input operating voltage range for $24V^{}_{\rm IN}$ and $48V^{}_{\rm IN}$ models

30W SINGLE

% FL	Minimum Input Operating Voltage			
	24V _{IN}	48V _{IN}		
10	7.0	14.0		
25	8.5	17.0		
50	8.8	18.0		
75	9.0	18.5		
100	9.5	19.5		



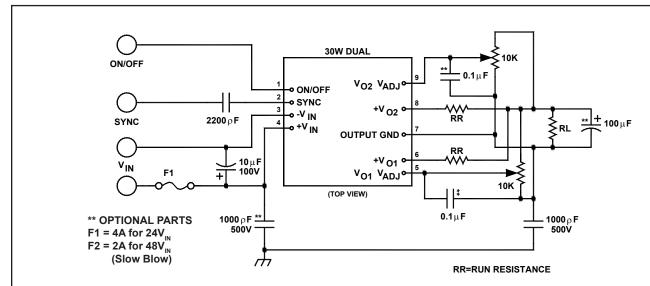


FIGURE 3. Parallel operation

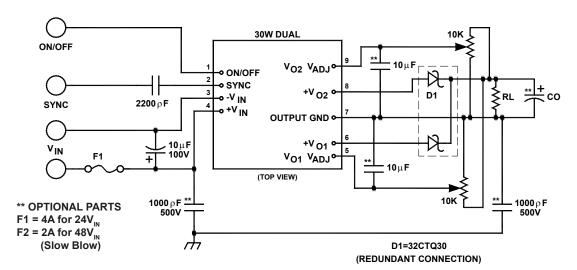


FIGURE 4. Redundant operation